

Figure 1 Traffic Node System Description

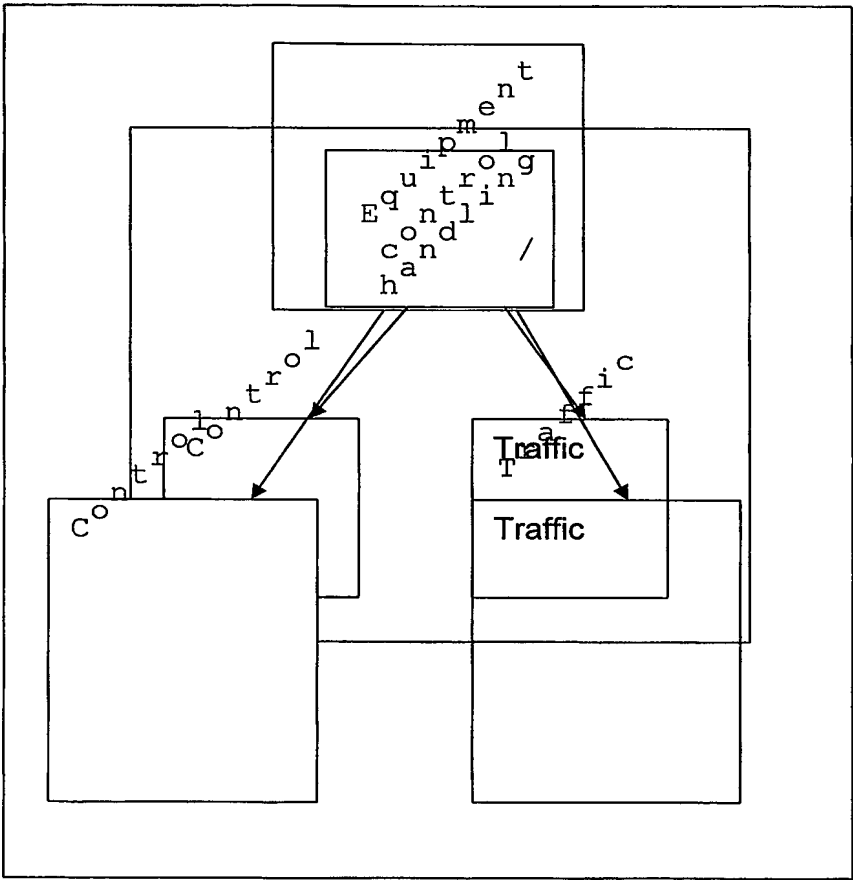


Figure 2 Application of the Traffic Node in the Lower Radio Access Network

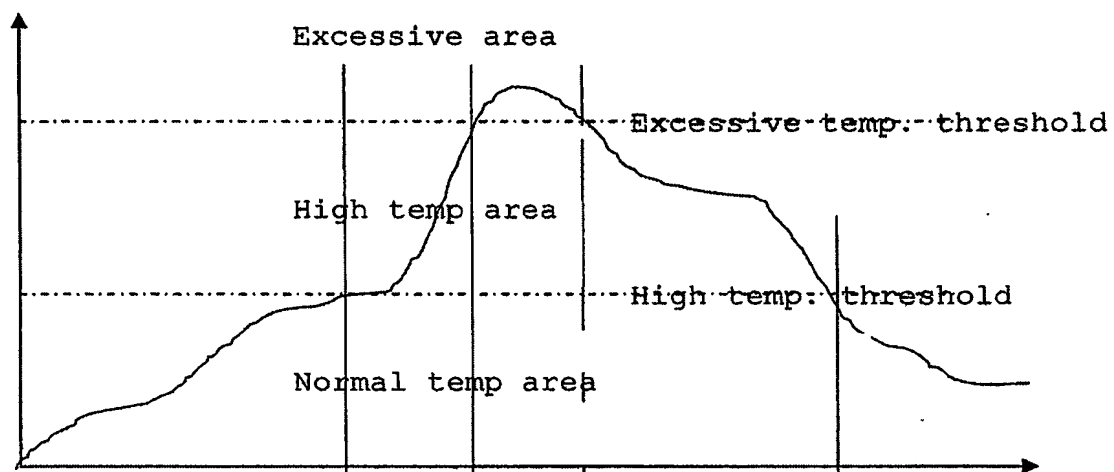


Figure 3 LTRAN network and the role of various Traffic Node sub-networks.

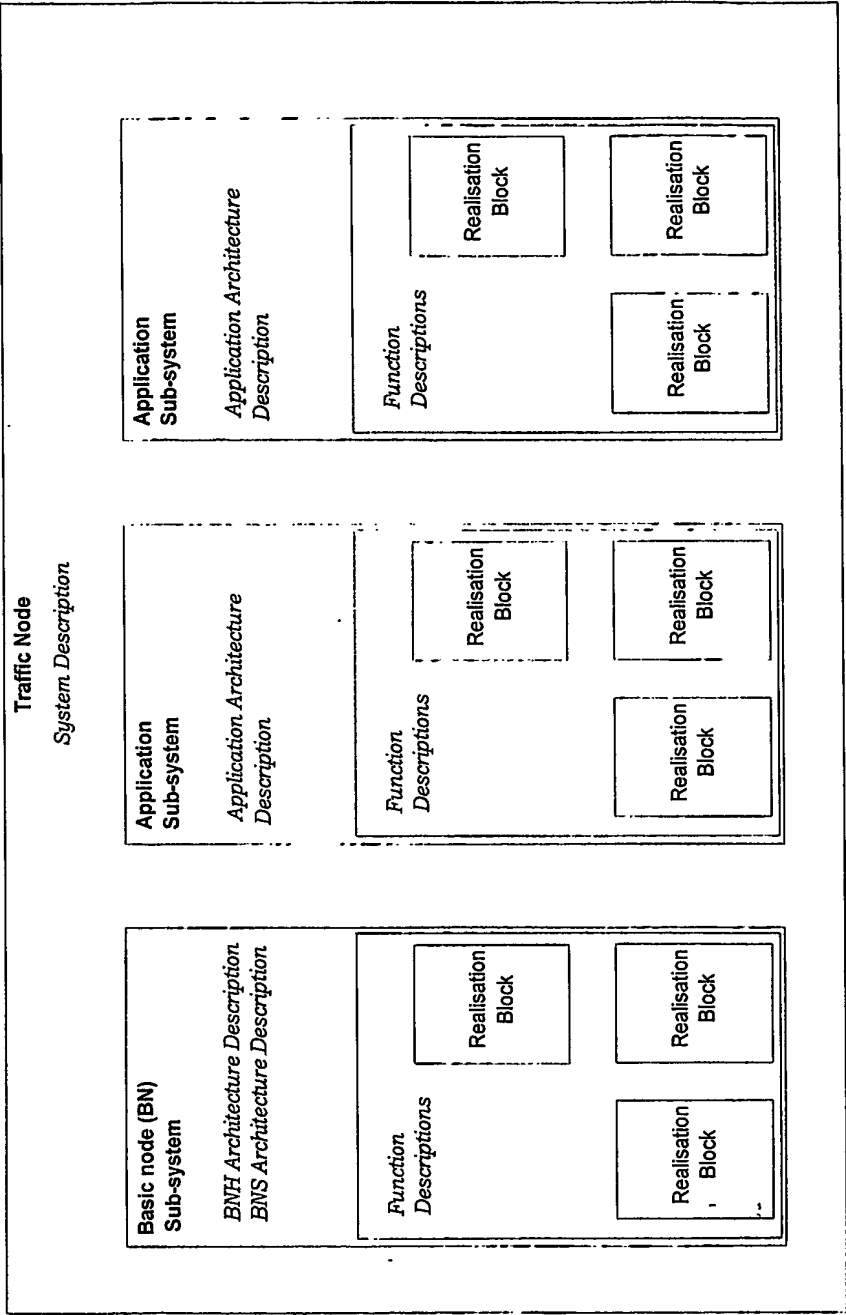


Figure 4 O&M environment of Traffic Node

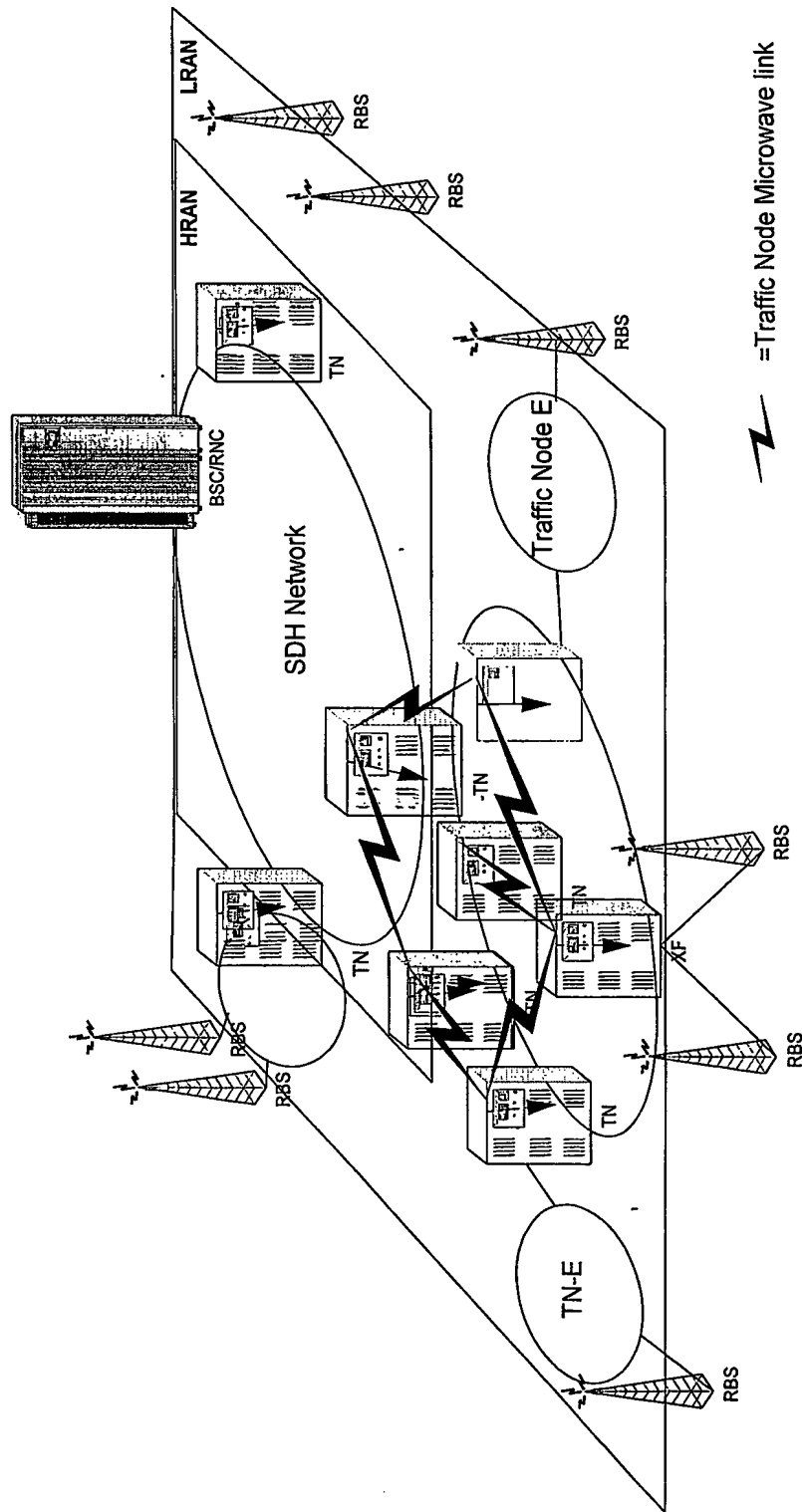


Figure 5 The TN IP based DCN

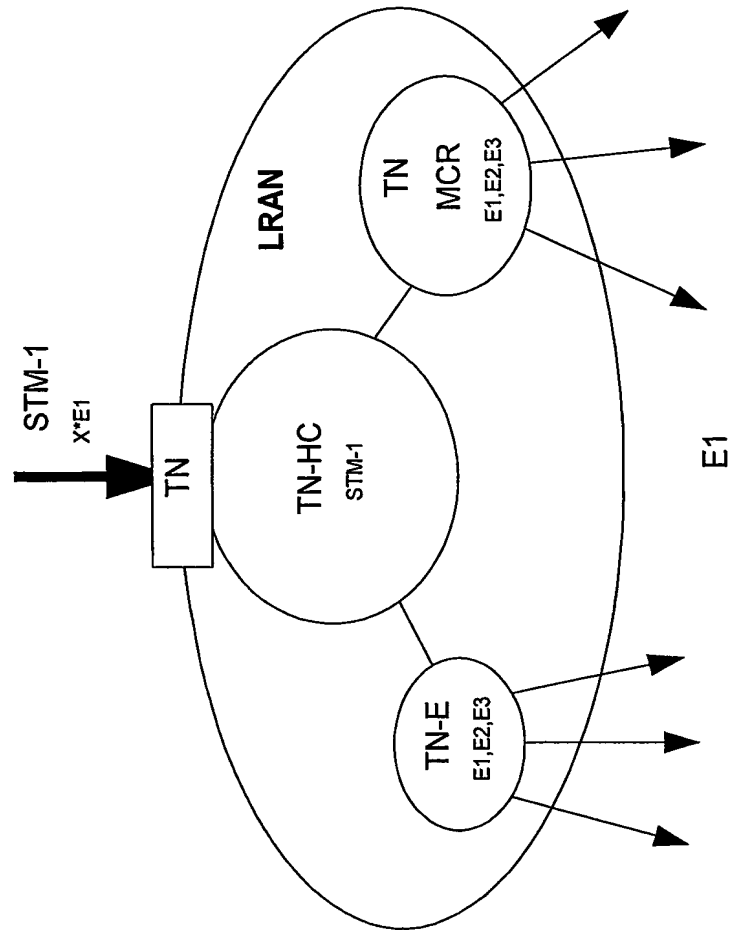


Figure 6 TN modularity

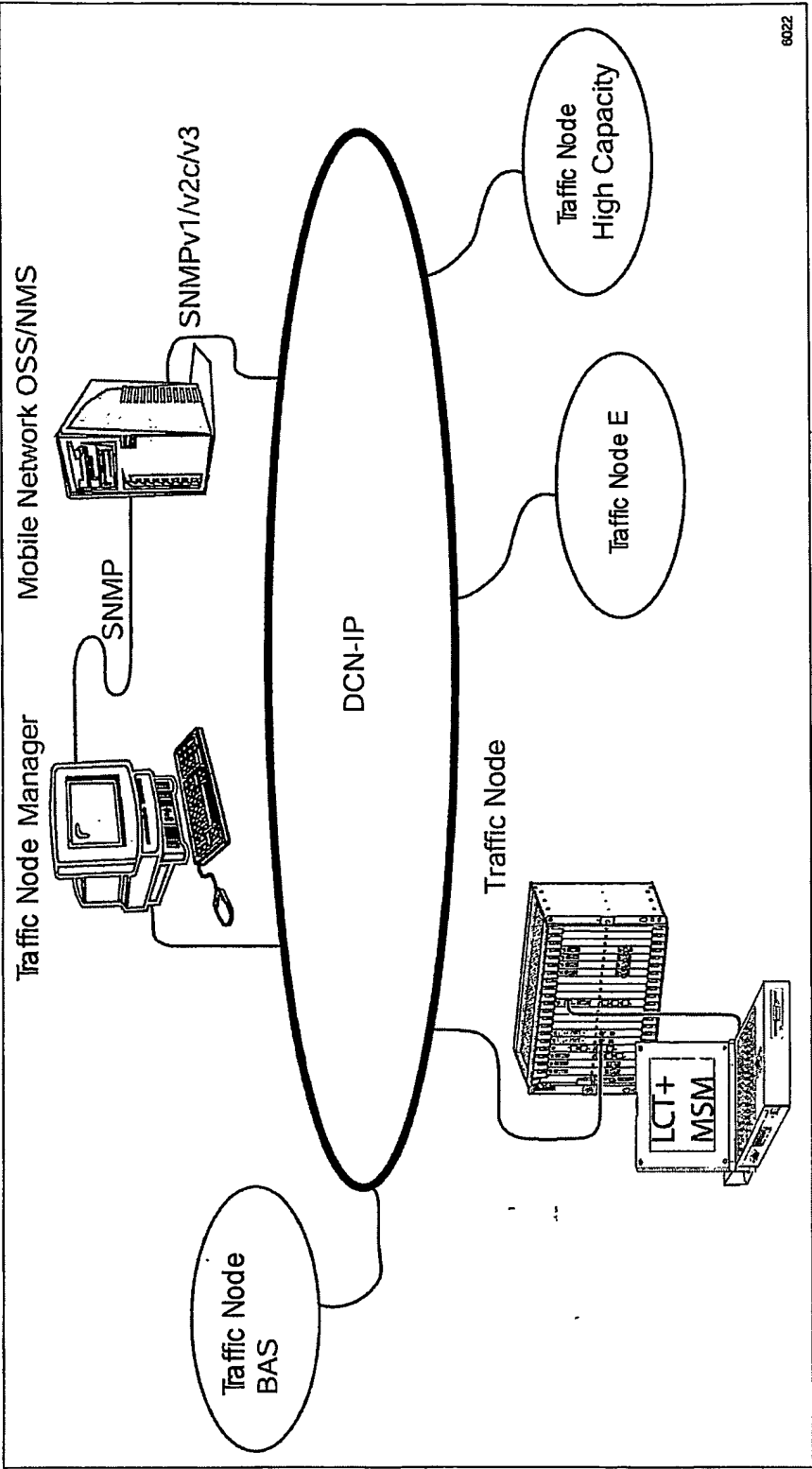


Figure 7 TN architecture

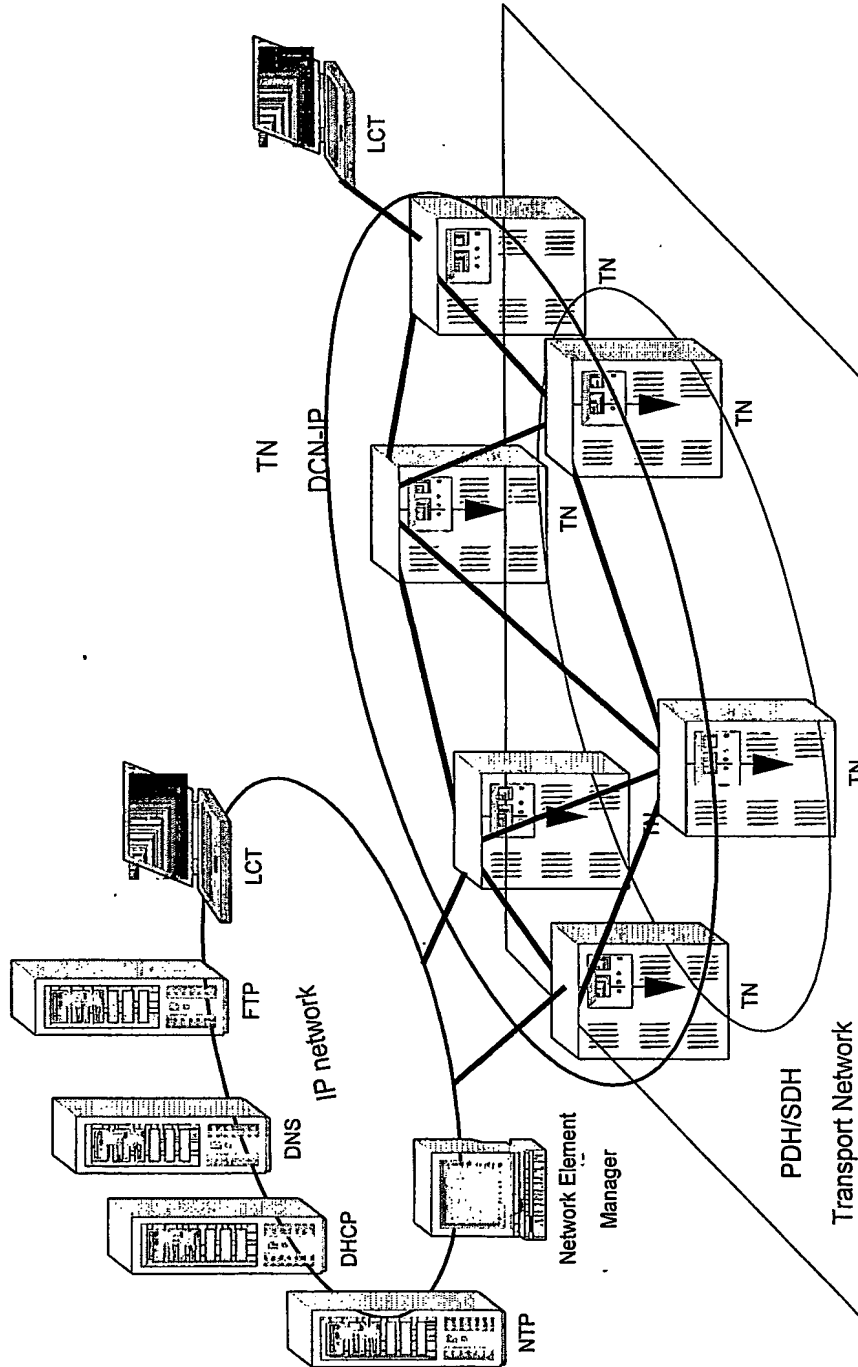


Figure 8 TN software architecture

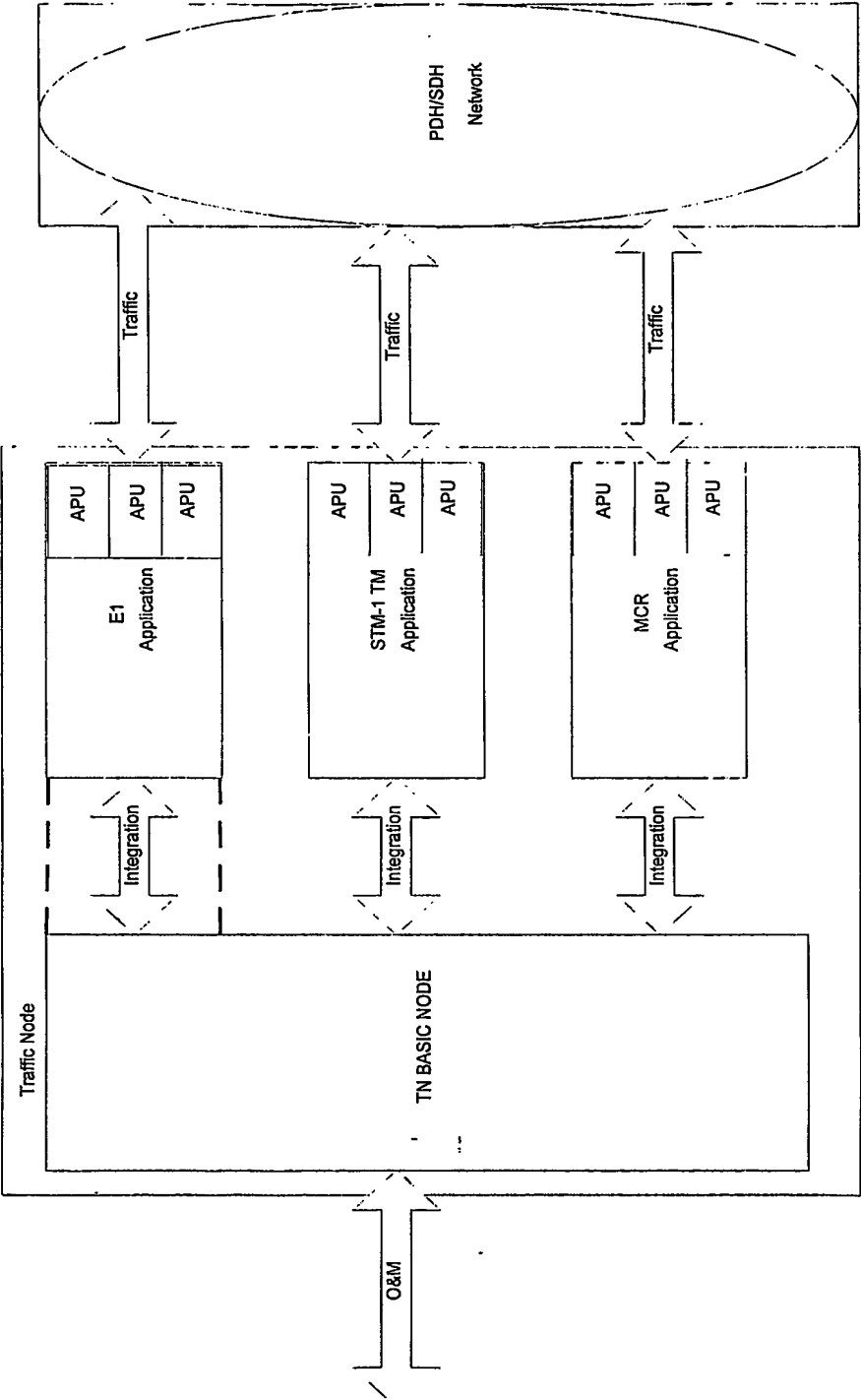


Figure 9 TN BNH busses and building blocks

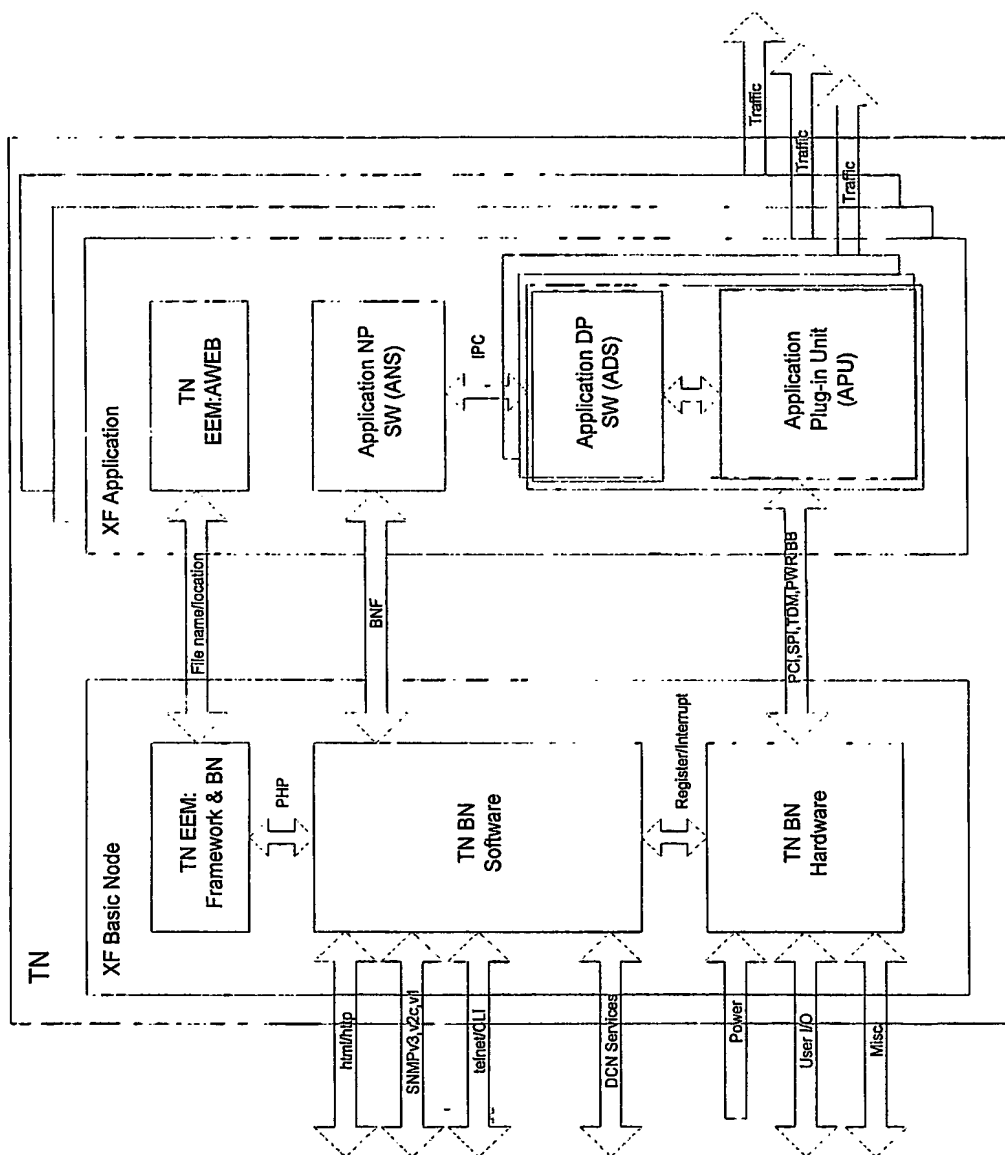


Figure 10 The TN AMM 20p Backplane

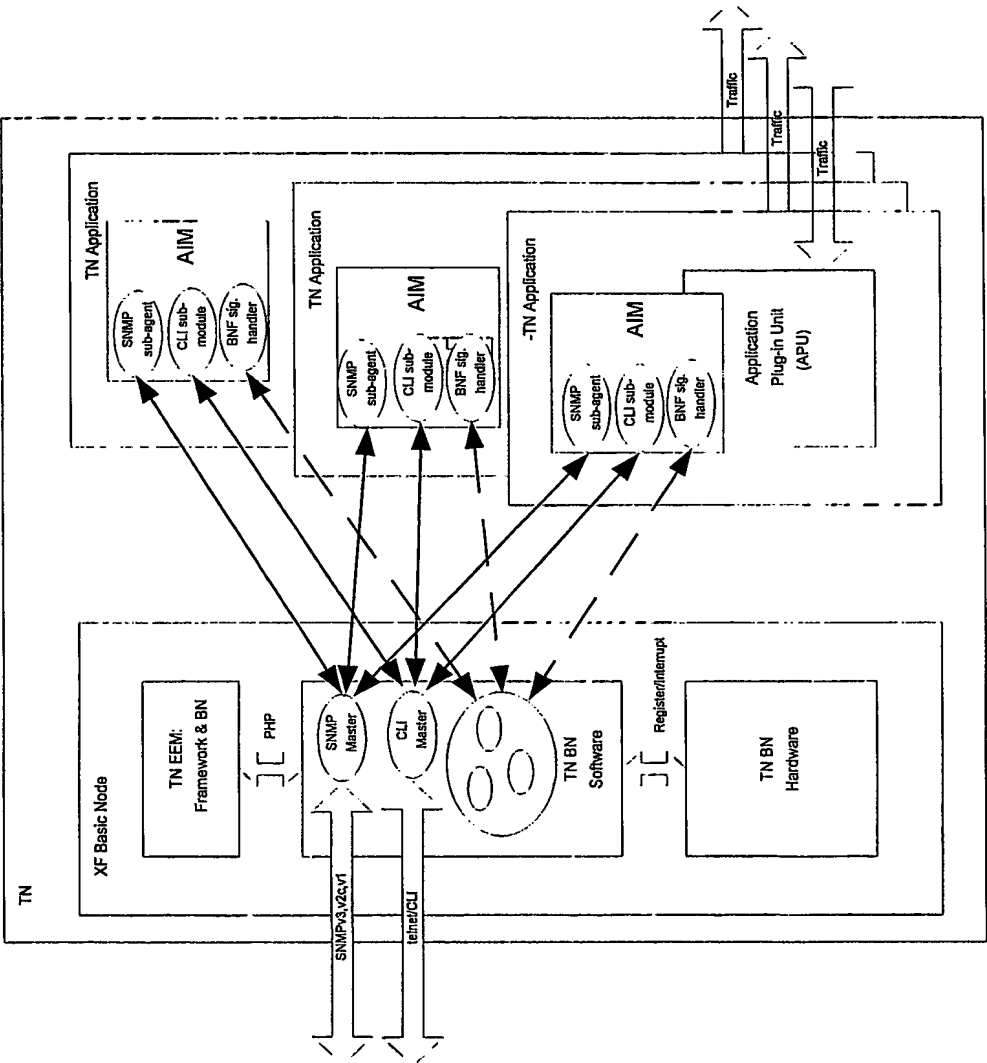


Figure 11 TN BNS

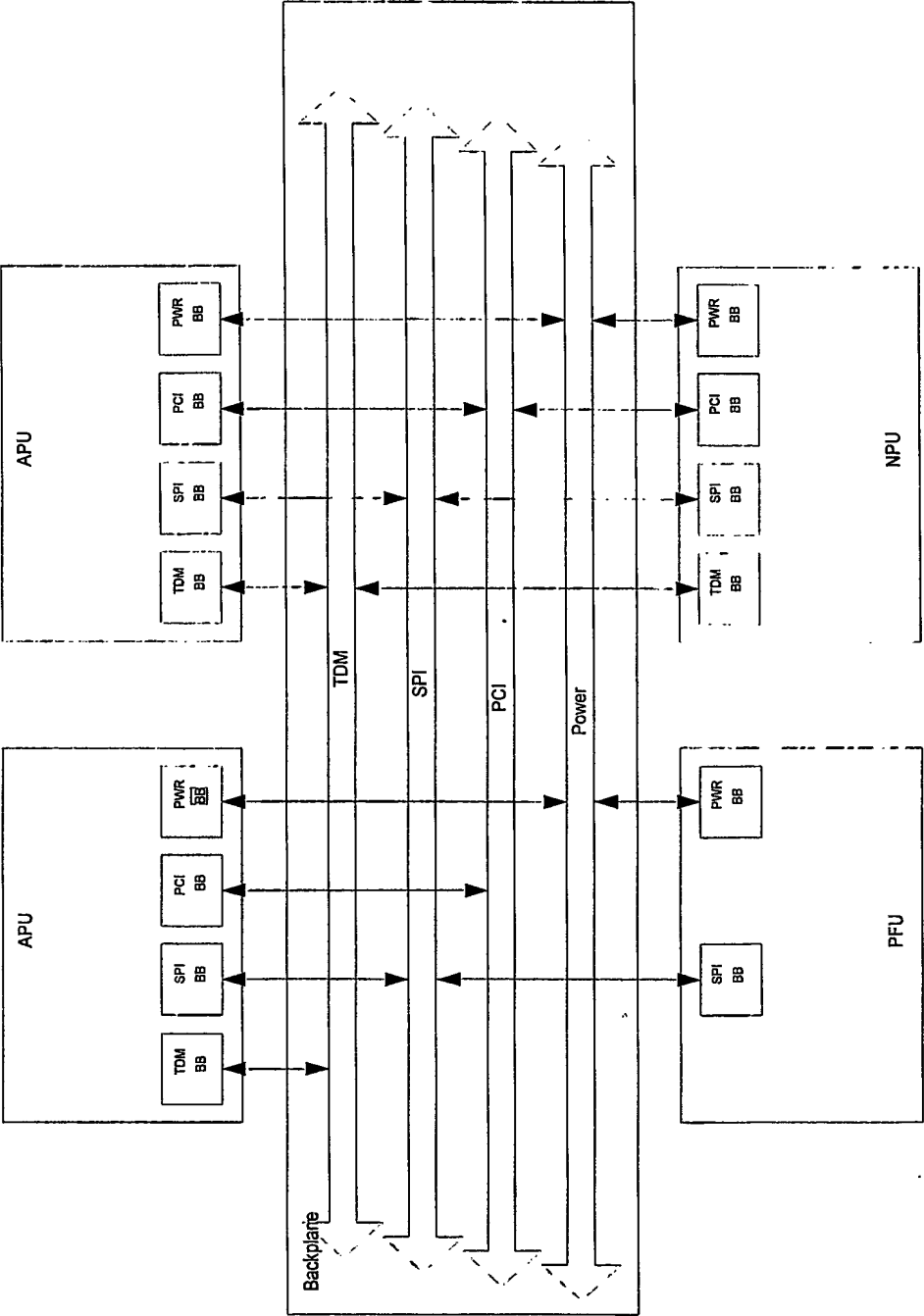


Figure 12 TN EEM: Framework and Basic Node

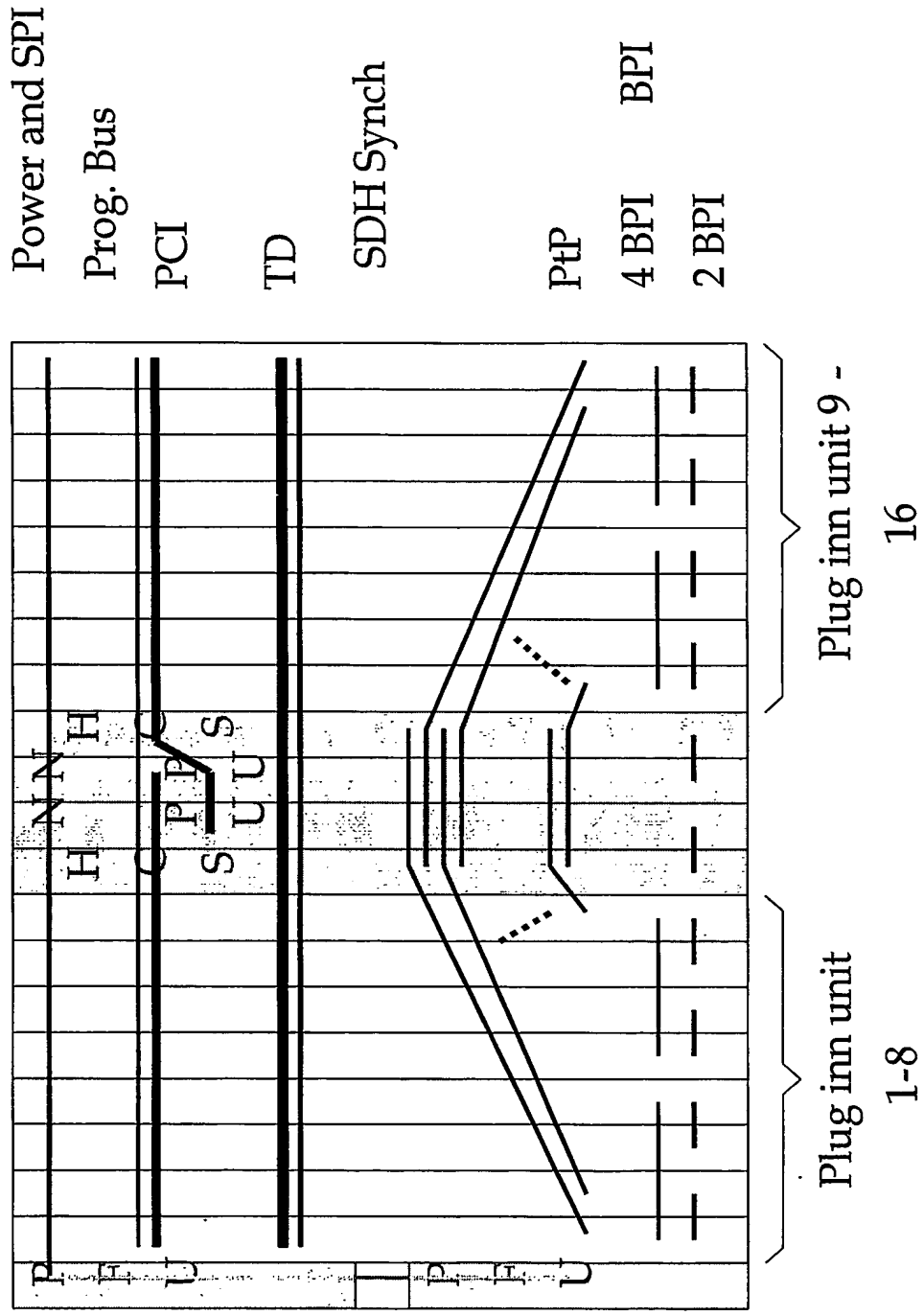


Figure 13 TN BNH

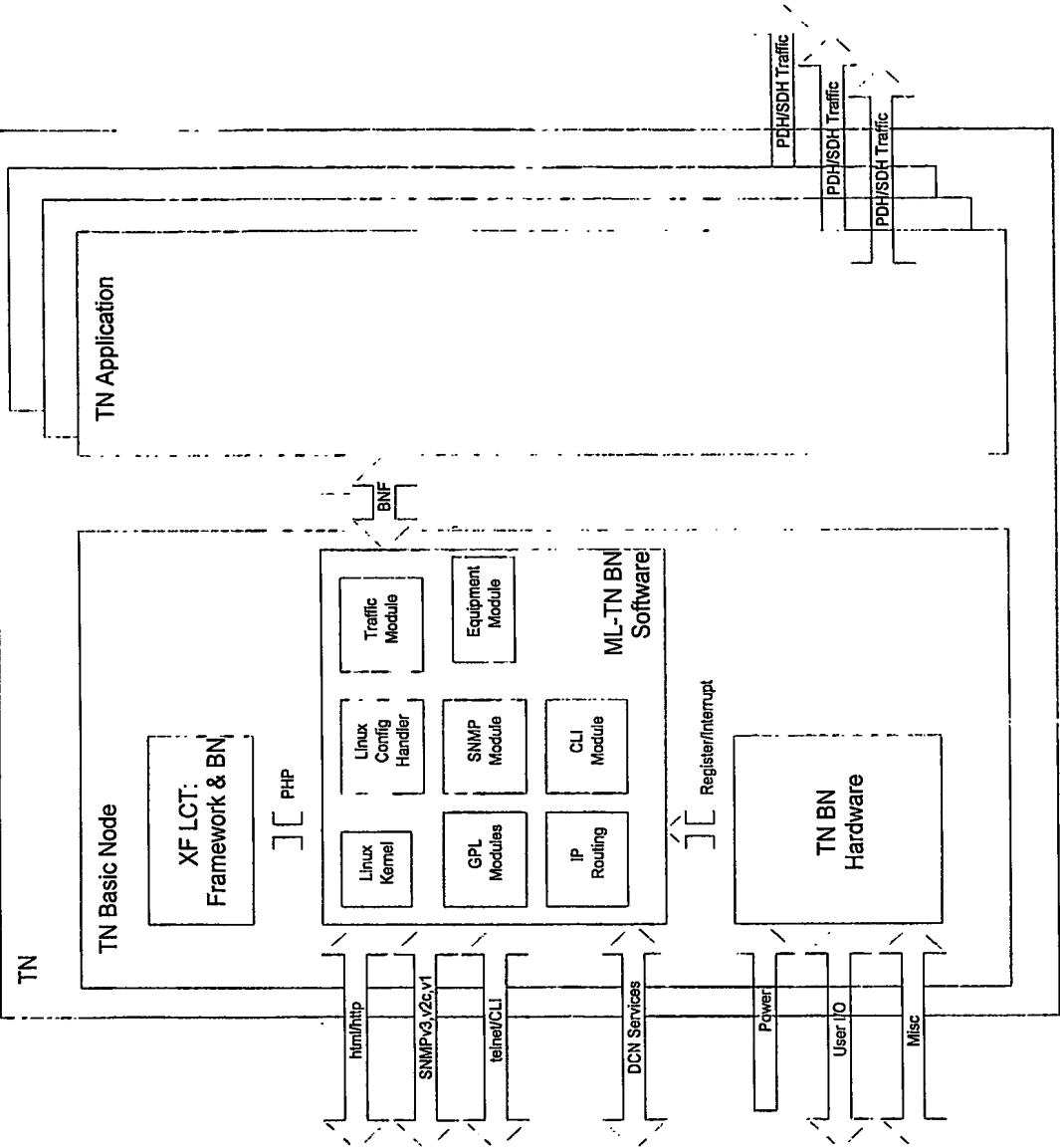


Figure 14 TN Application architecture

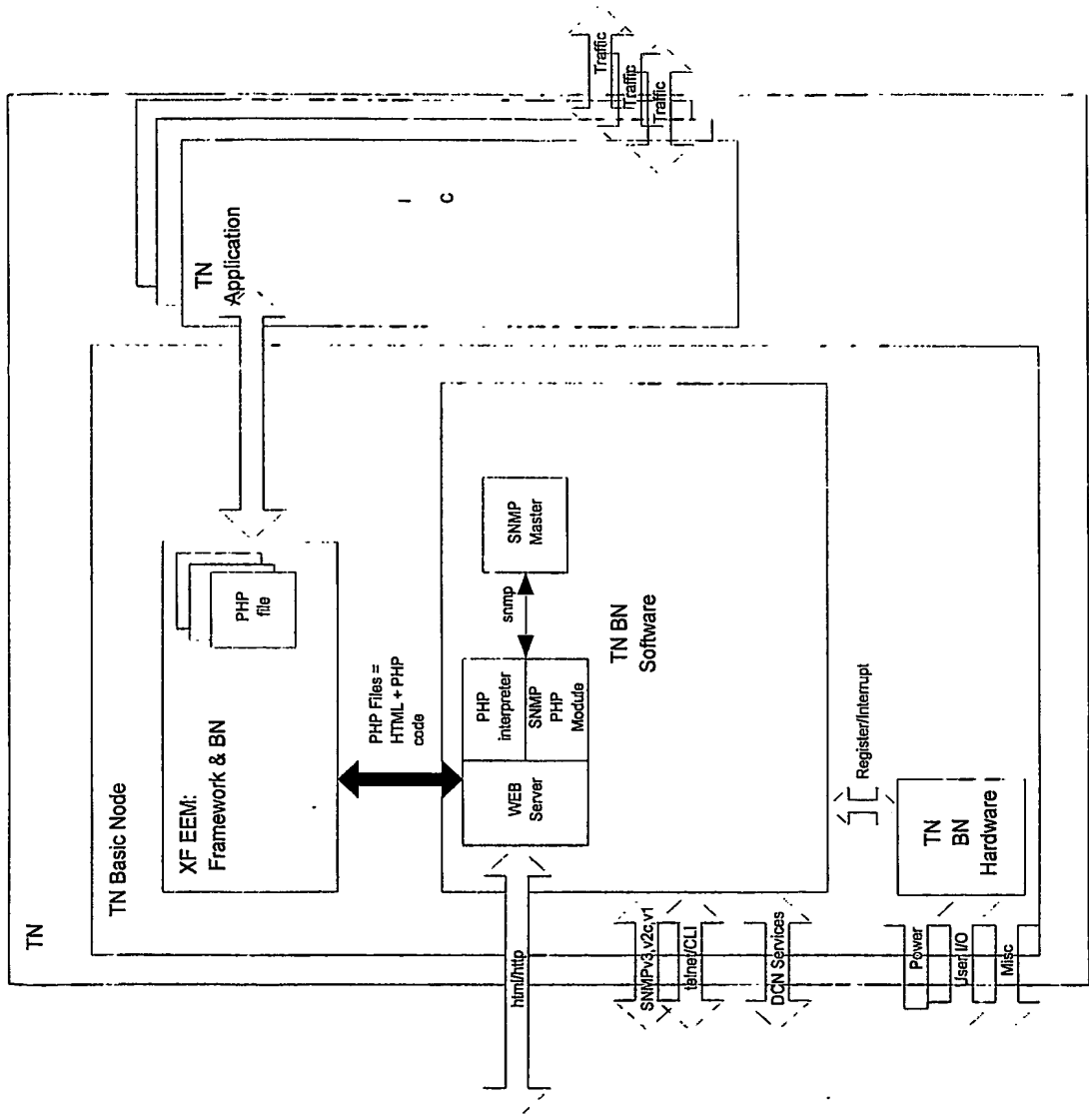


Figure 15 TN Application Software

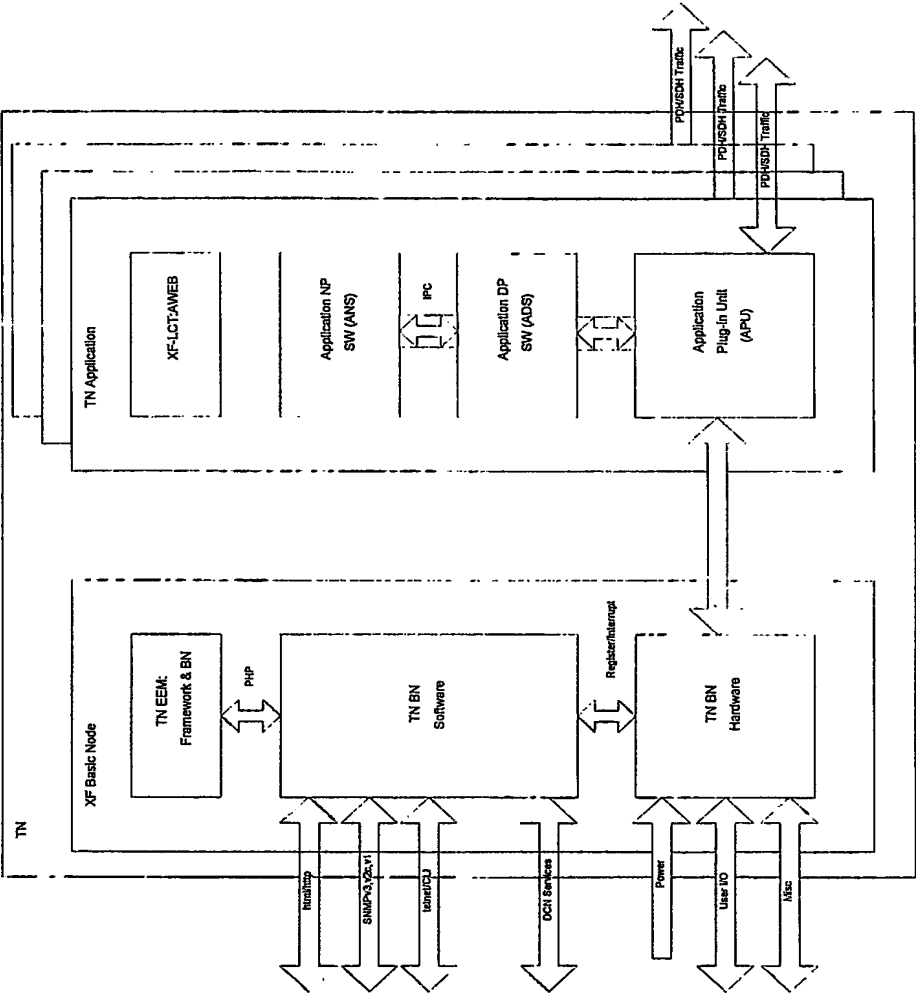


Figure 16 TN ANS architecture

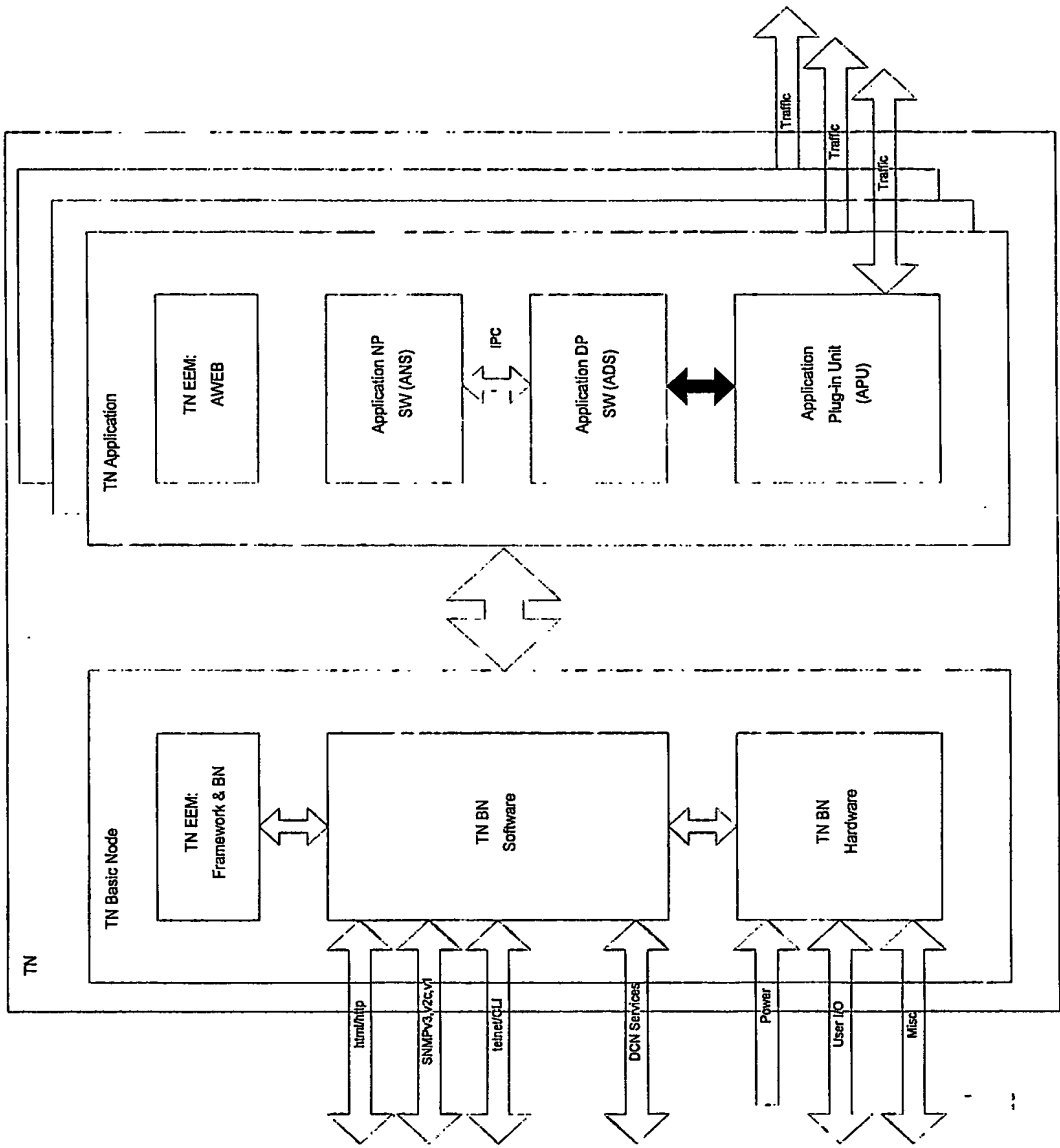


Figure 17 TN Application EEM

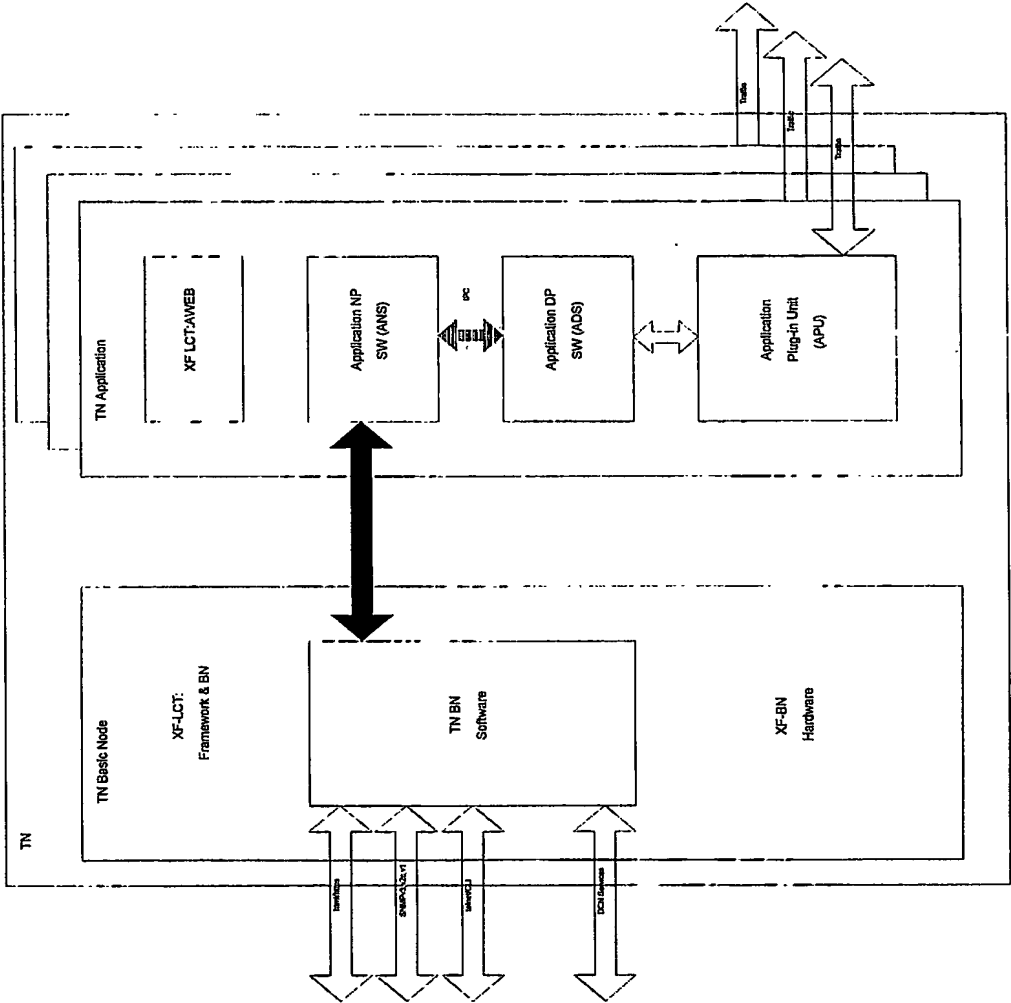


Figure 18 TN Application Hardware

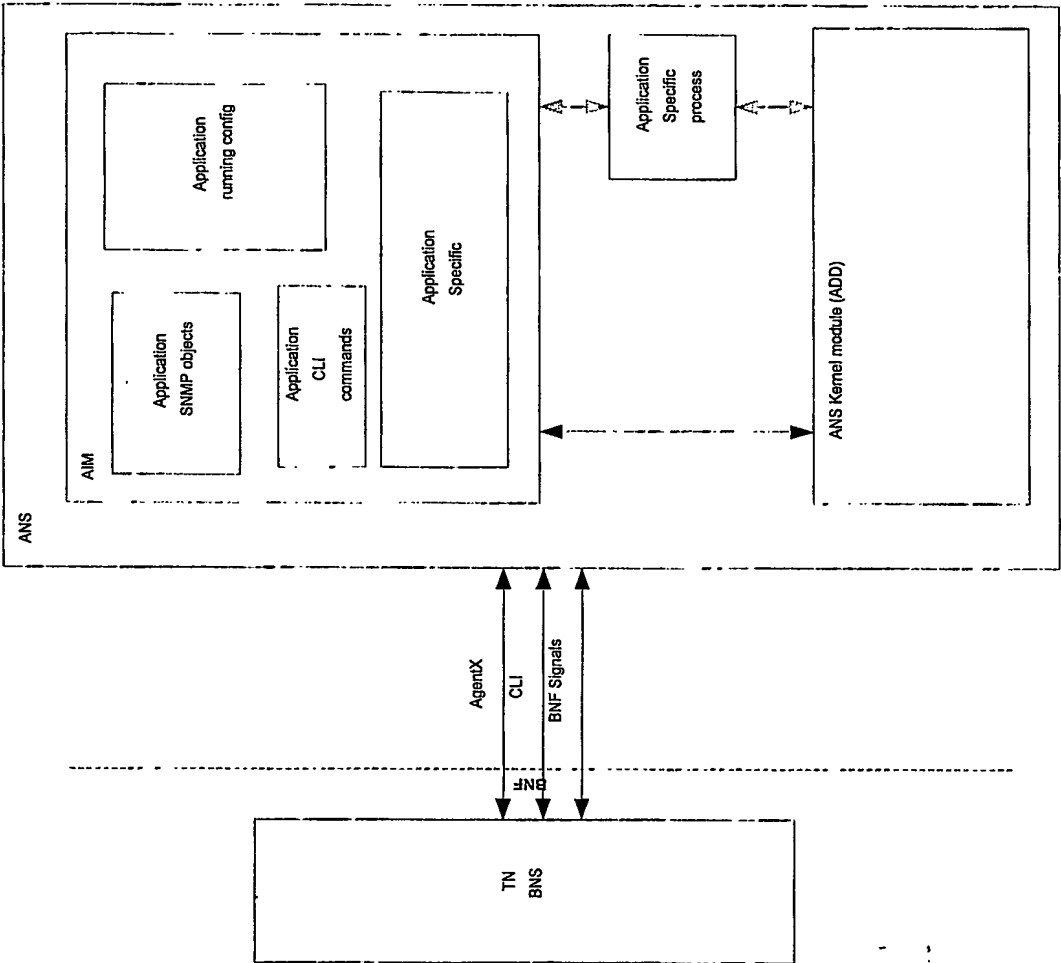


Figure 19 TN APU

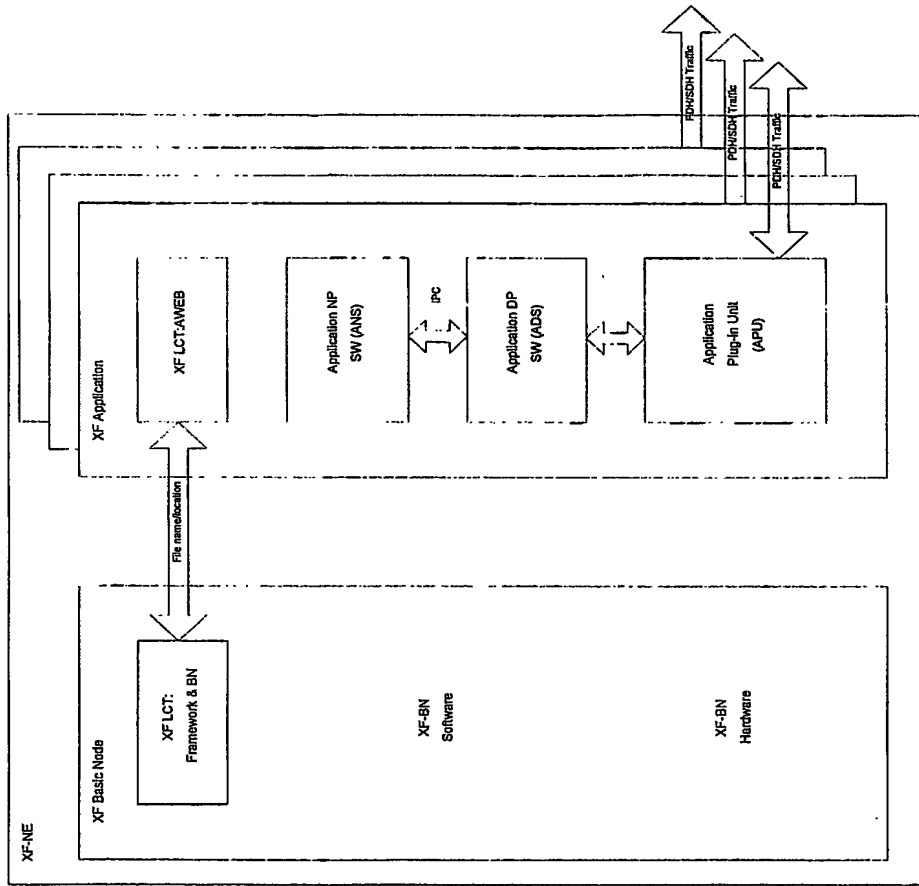


Figure 20 Example of a bi-directional 3*64Kbs cross-connection between the two APUs

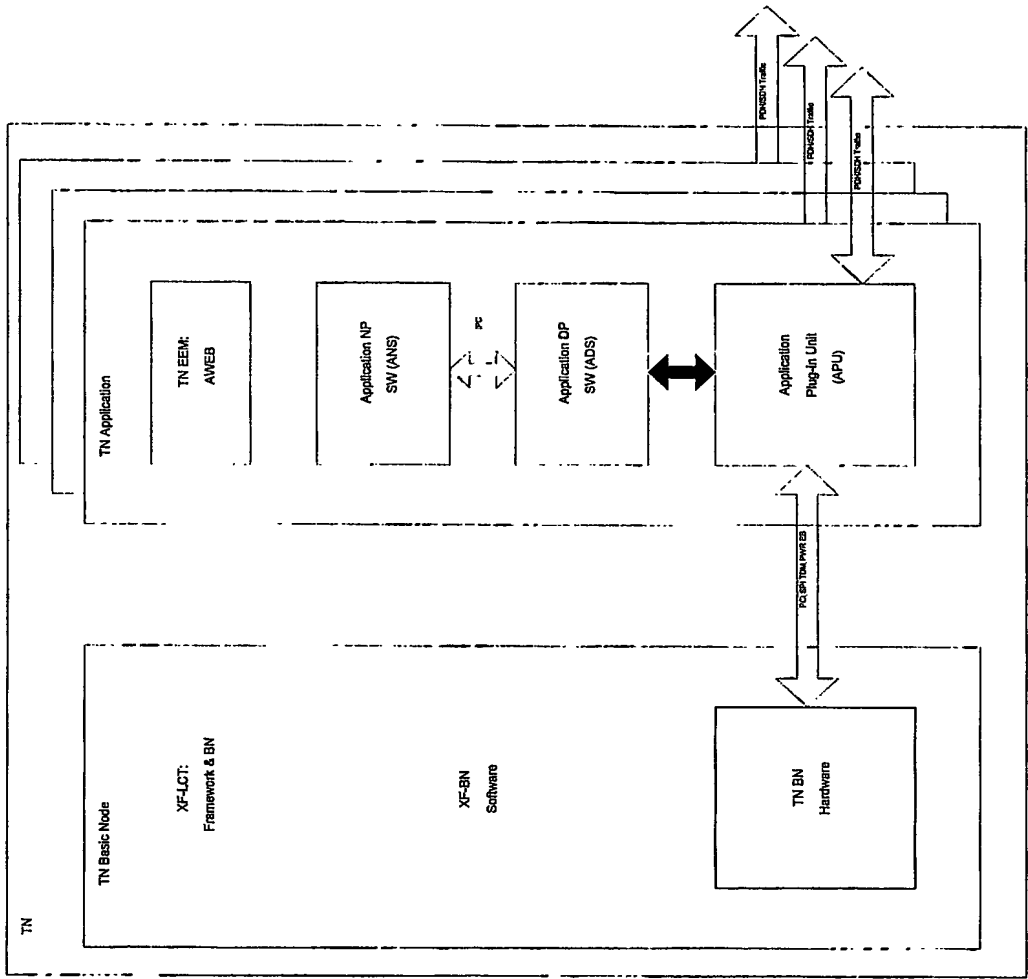


Figure 21 PM handling in TN

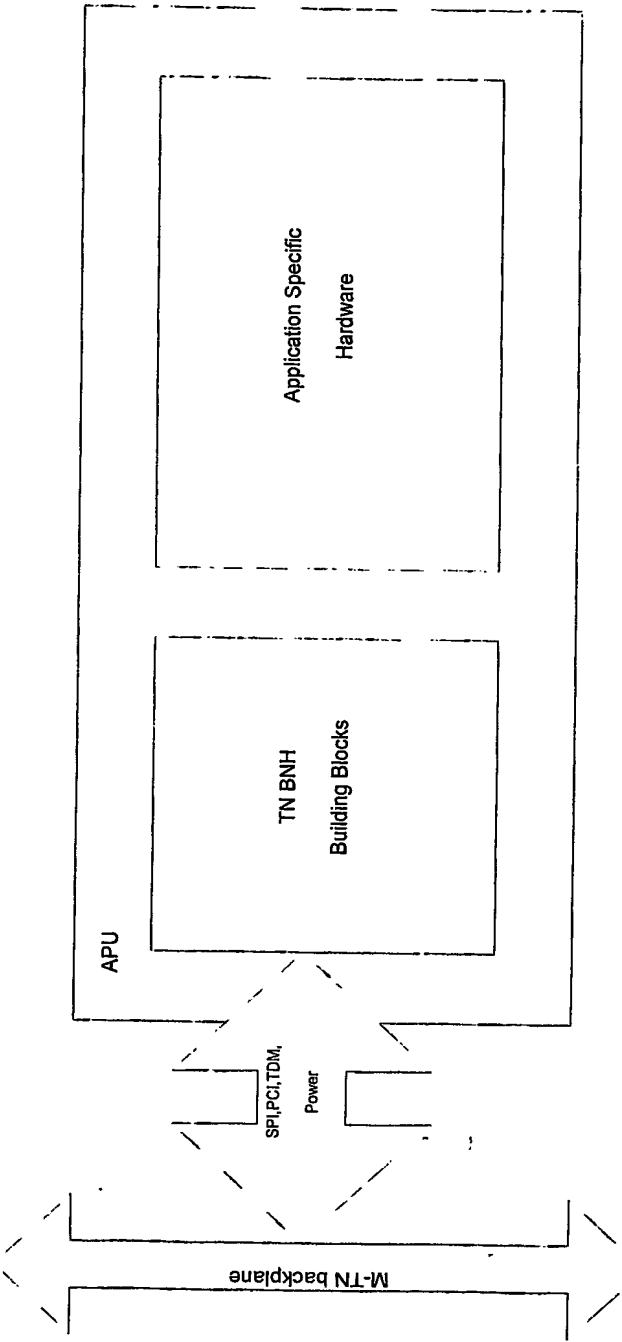


Figure 22 TN Alarm Handling overview

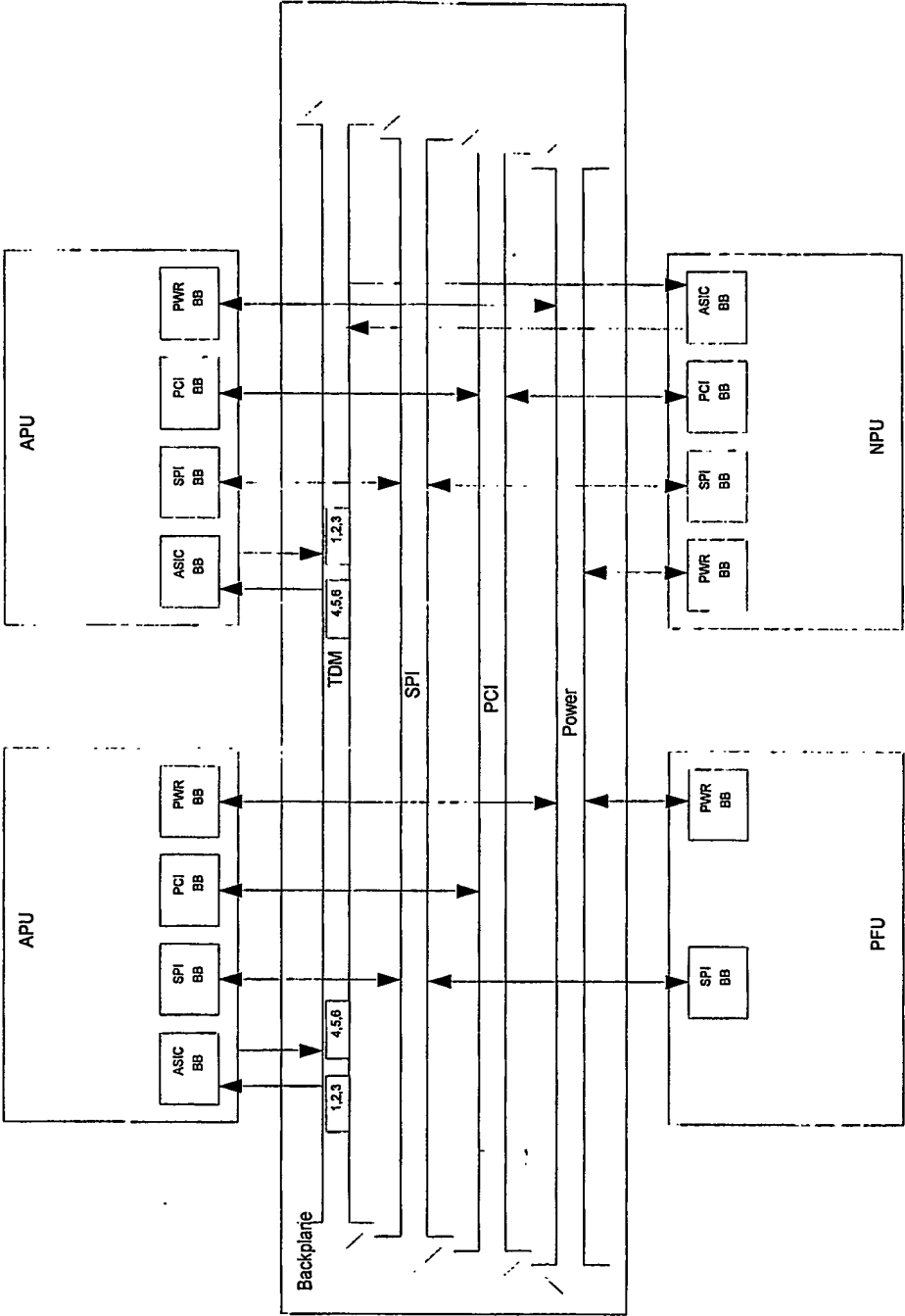


Figure 23 E1 carried on one interface.

BNS and ANS uses BNF messages.

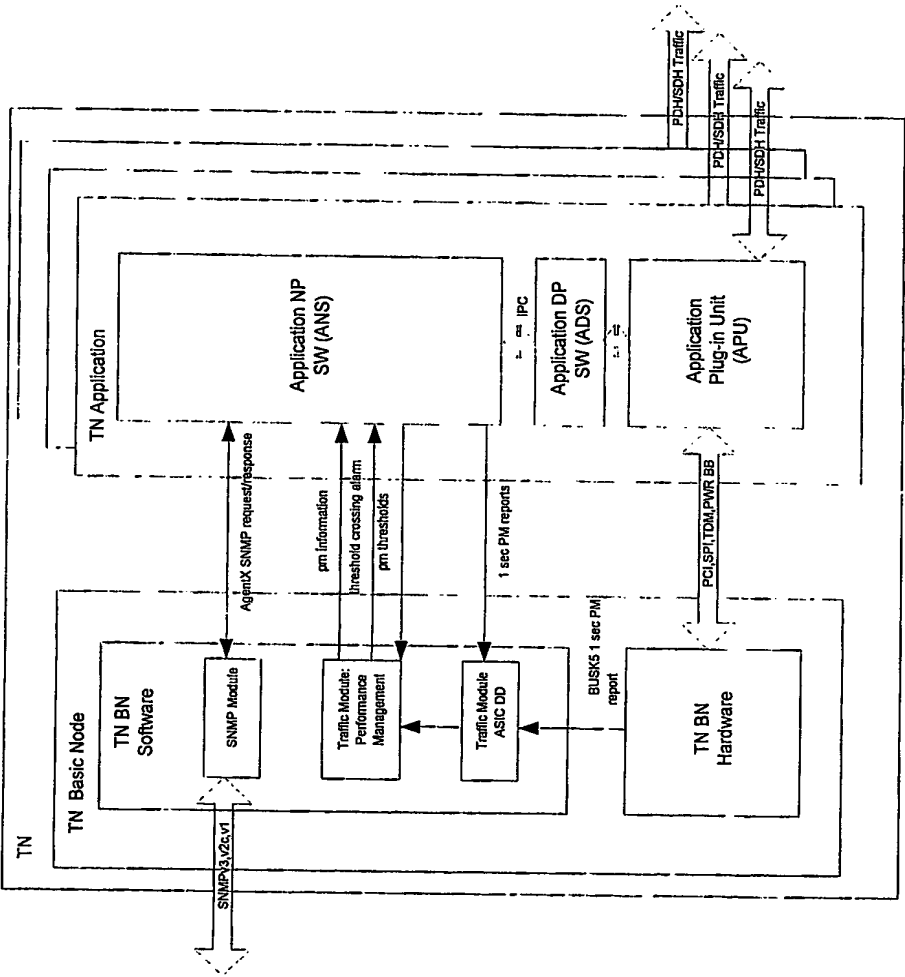


Figure 24 E1 carried on a terminal

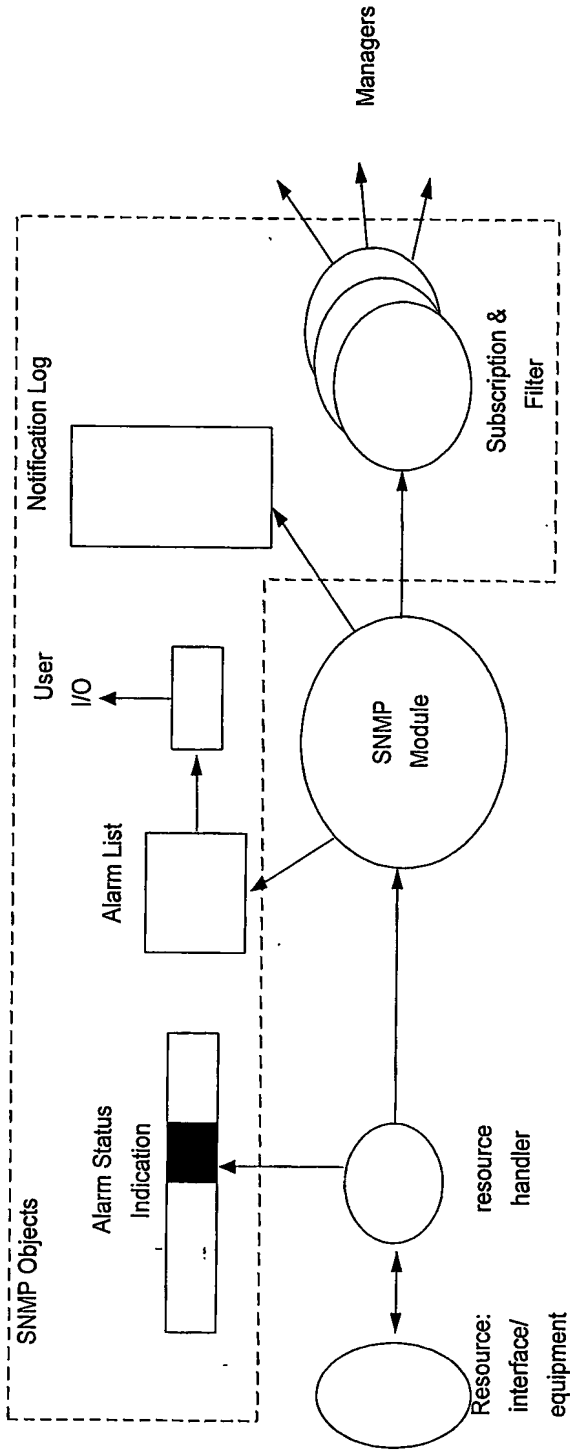


Figure 25 Redundancy model - basis for calculations

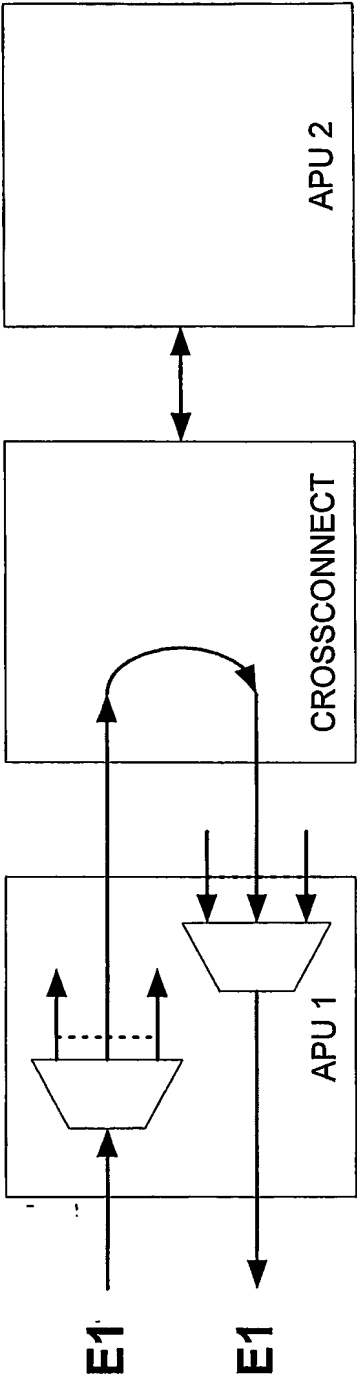


Figure 26 PIU function blocks

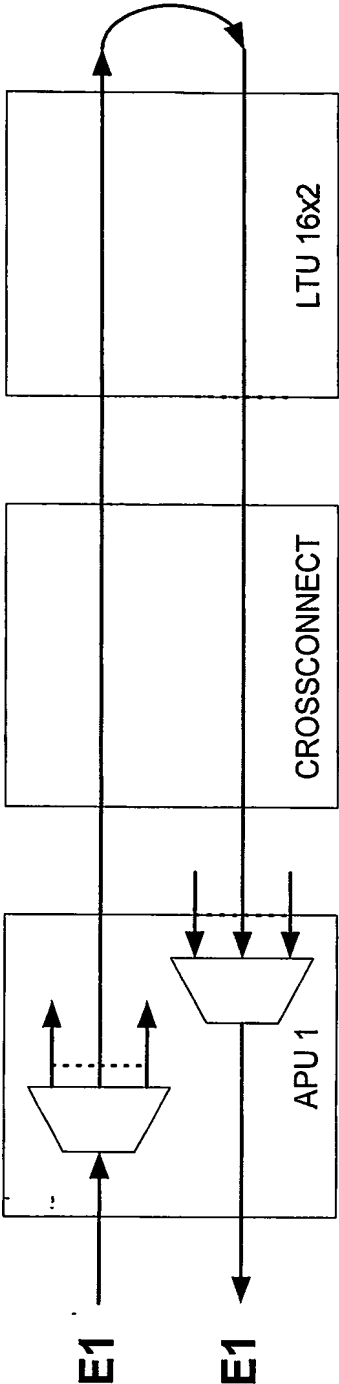


Figure 27 ASIC block structure

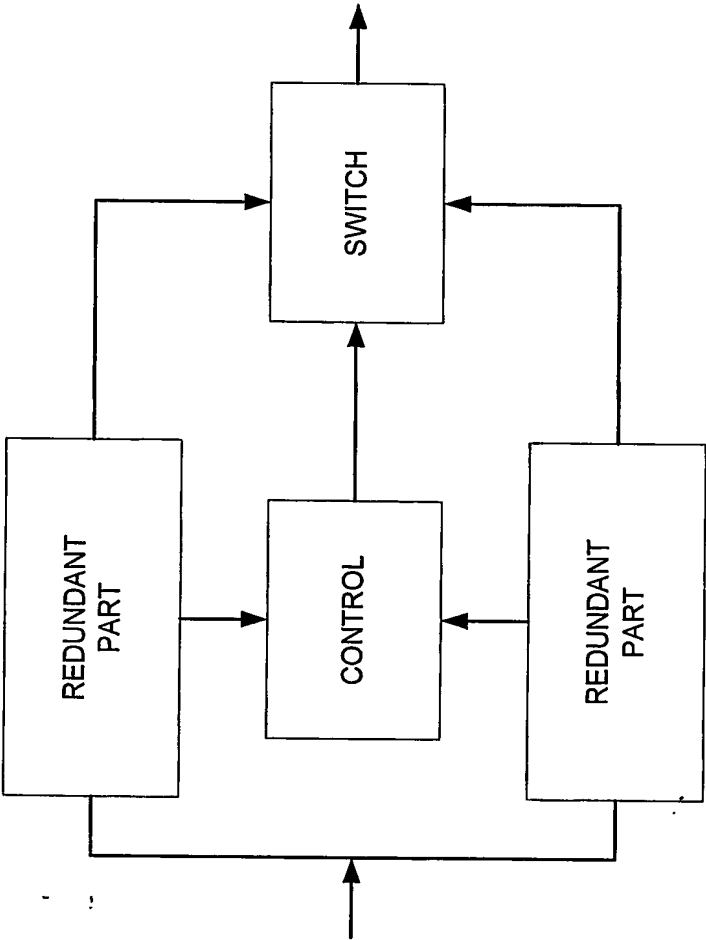


Figure 28 TDM bus redundancy

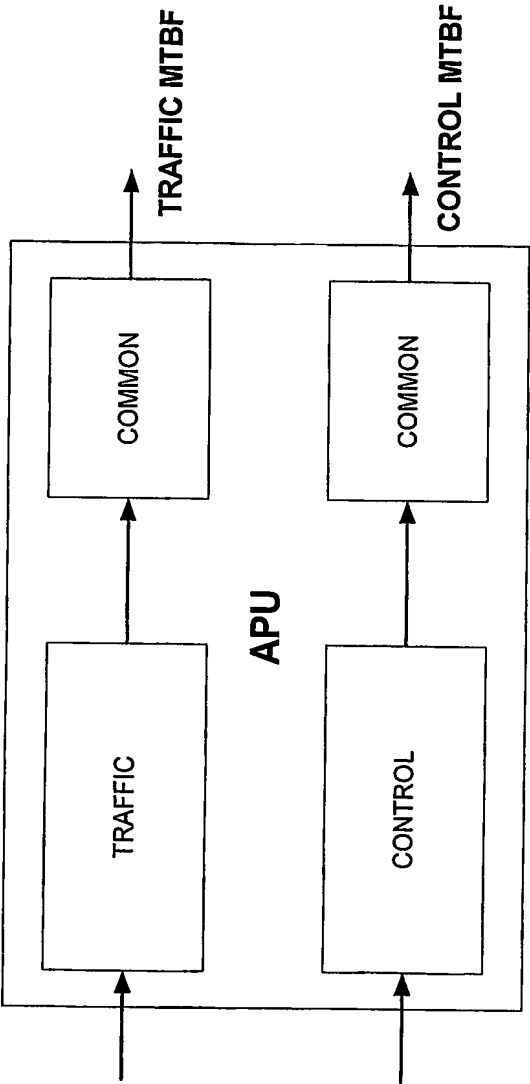


Figure 29 AMM 20p with redundant power distribution

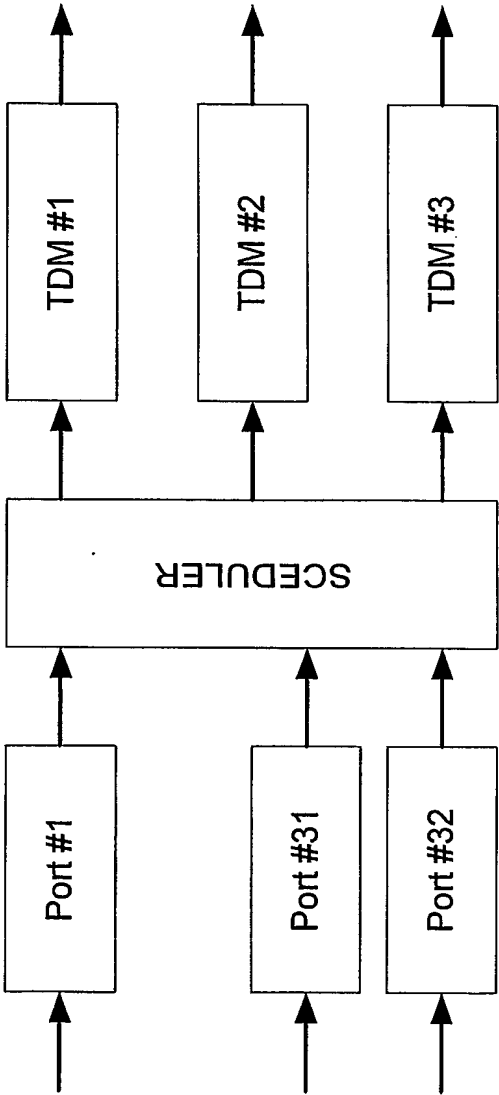


Figure 30 AMM 20p without redundant power distribution

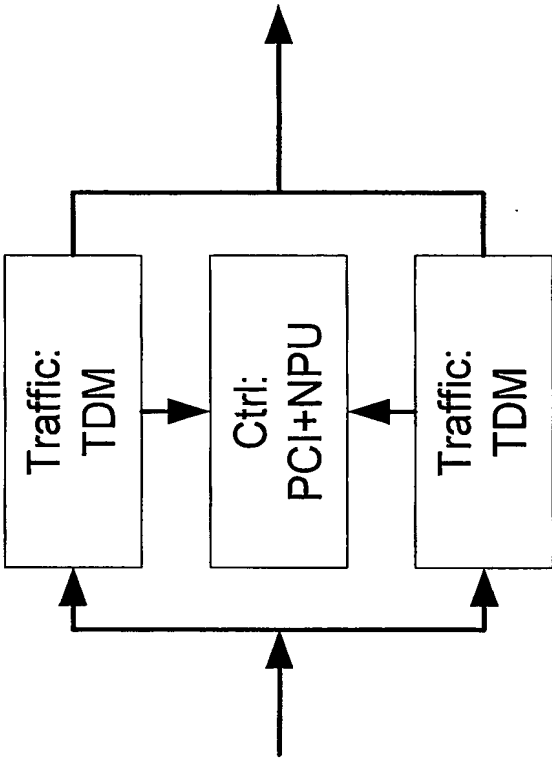


Figure 31 AMM 6p BN

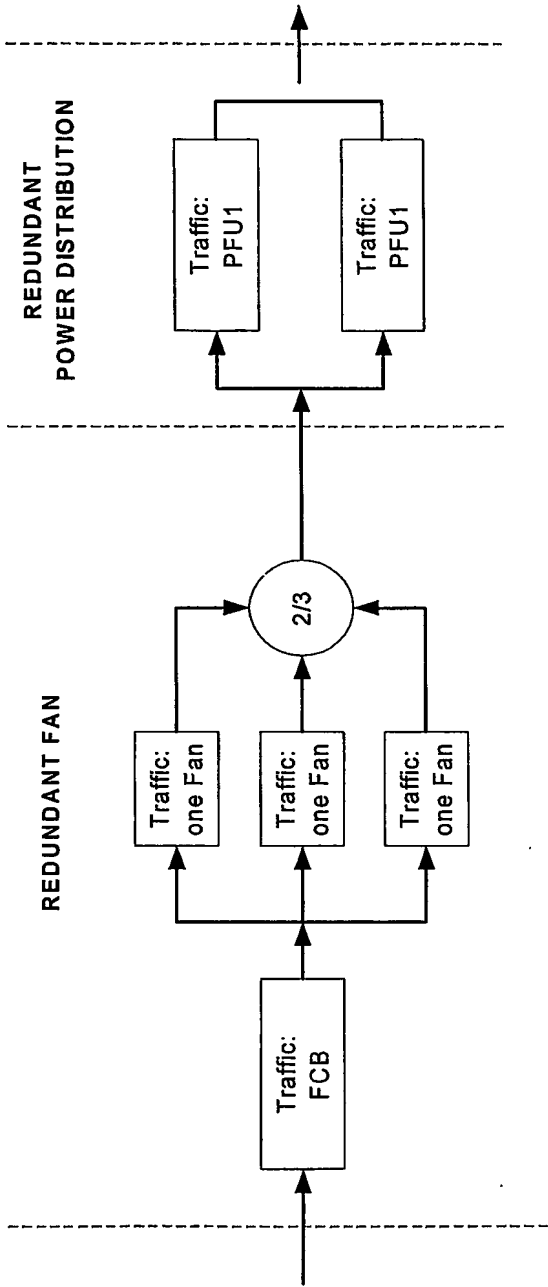


Figure 32 General model for protected interfaces

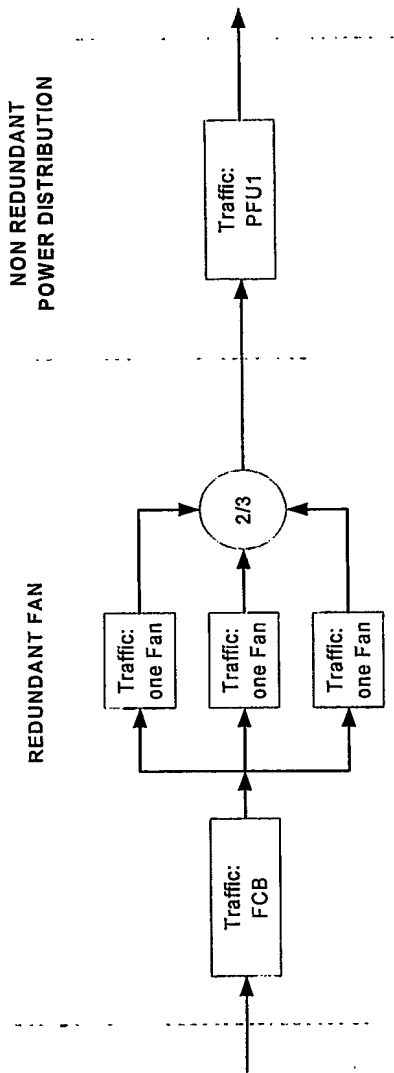


Figure 33 Simplified model for protected interfaces

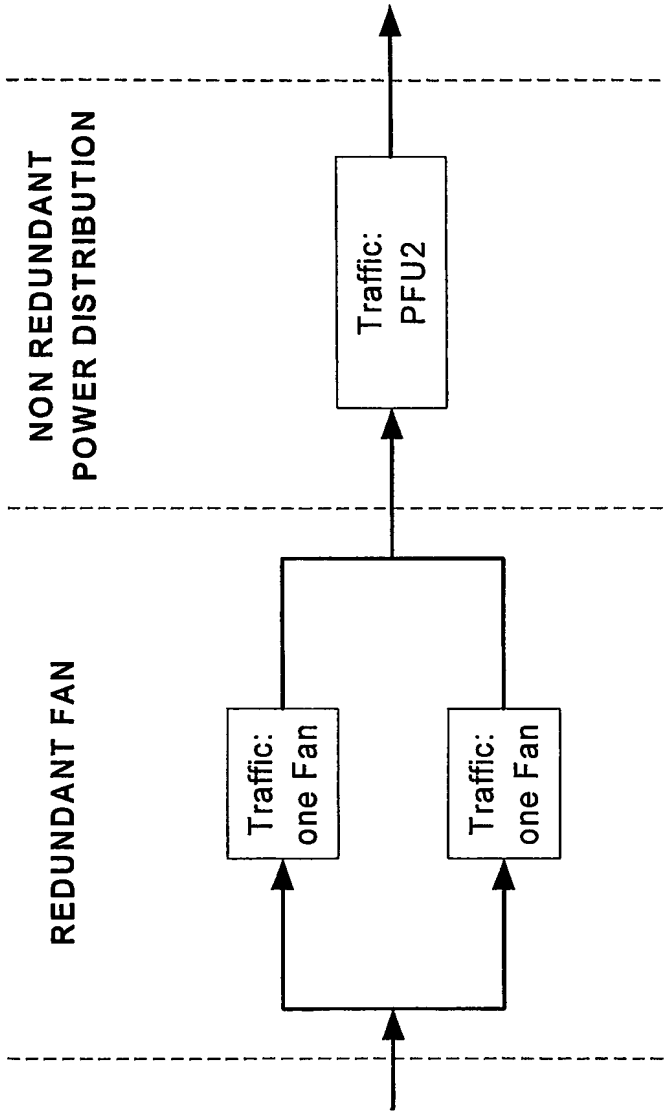


Figure 34 General model - unprotected interfaces

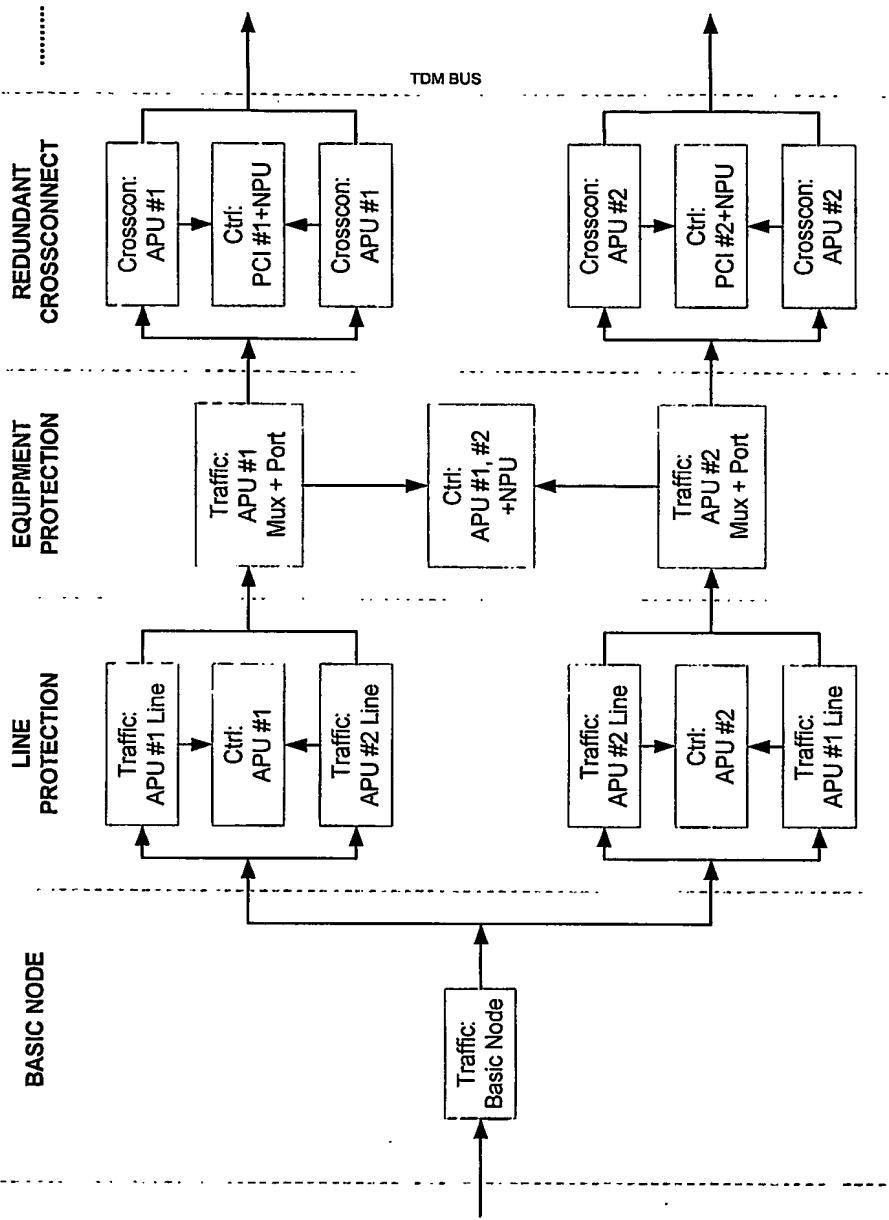


Figure 35 MCR 1+1

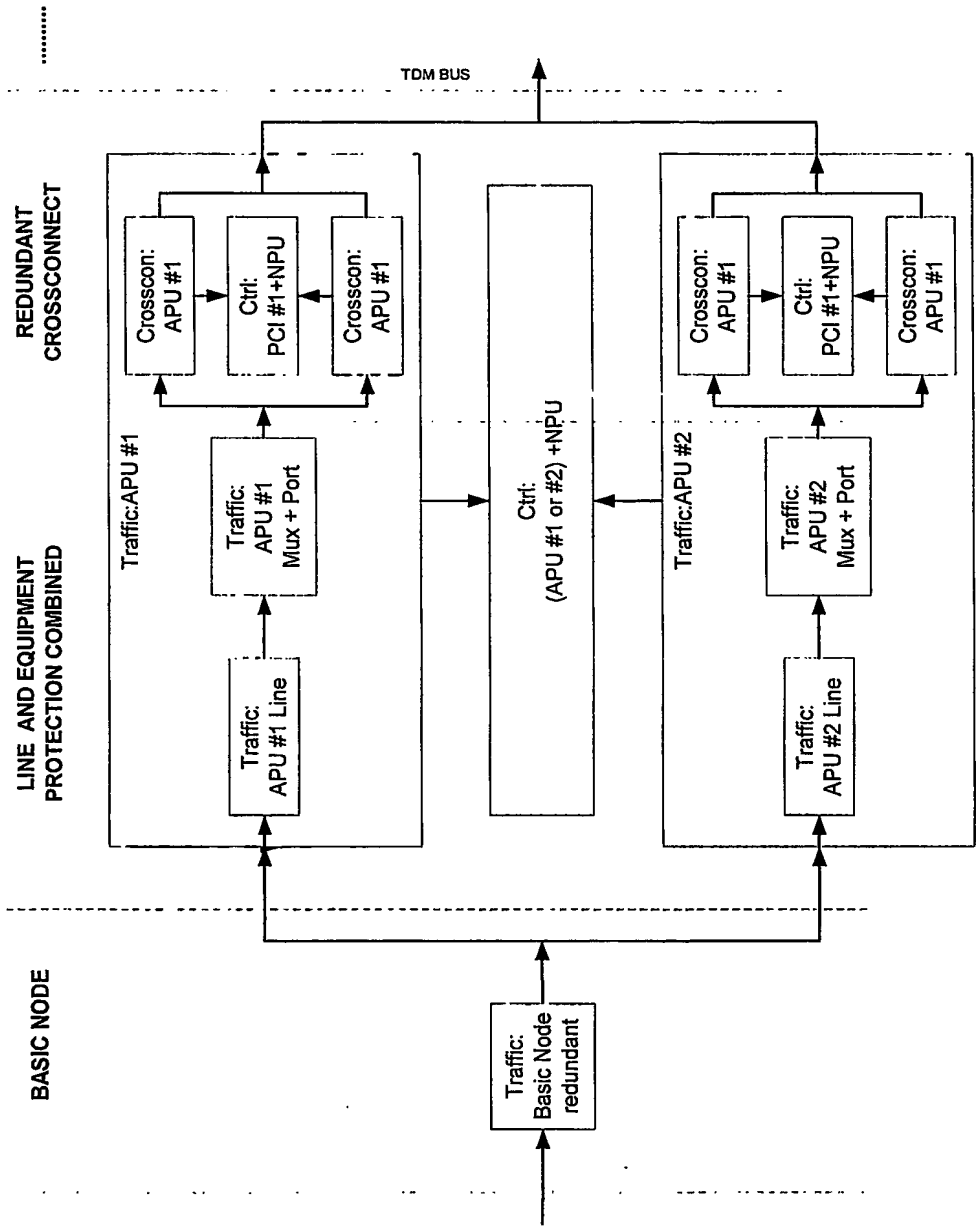


Figure 36 MCR 1+0

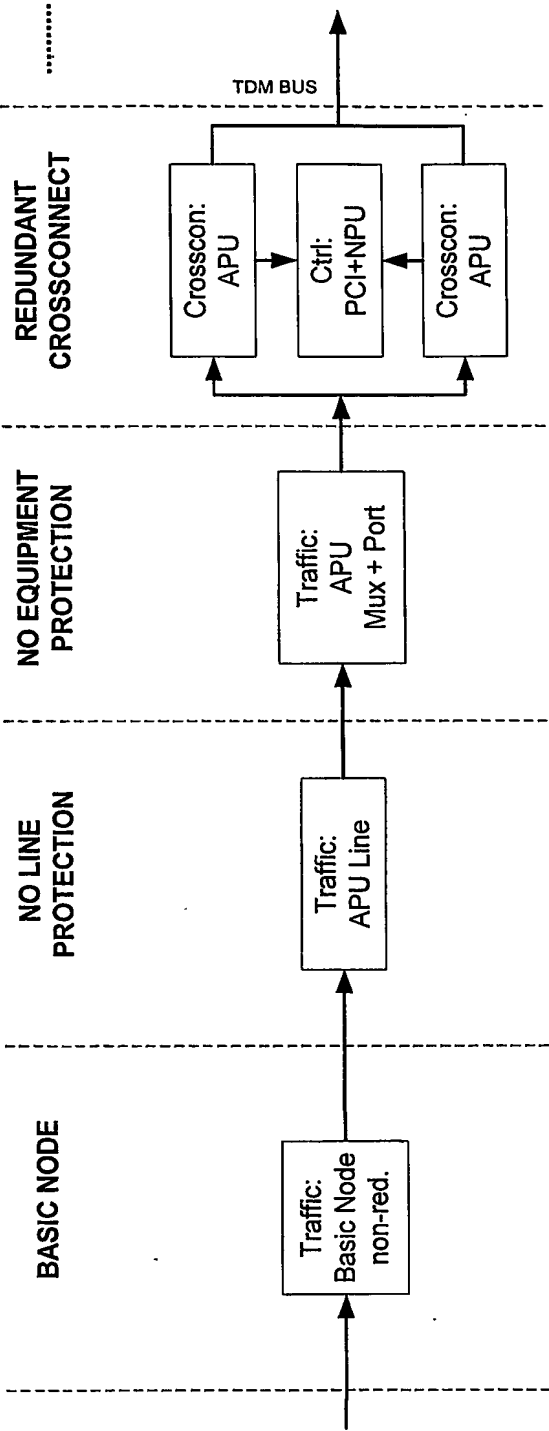


Figure 37 MCR terminal 1+1

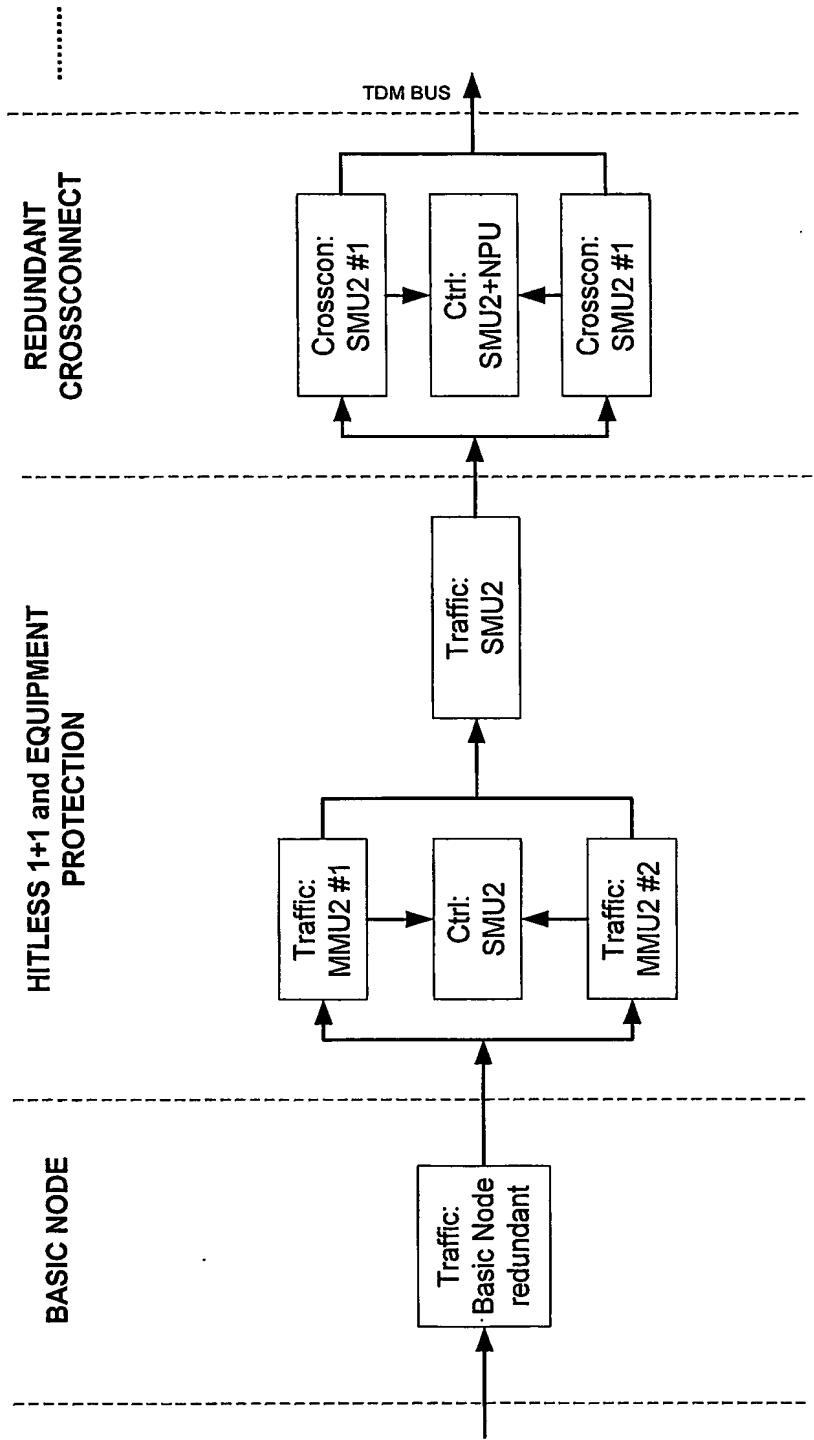


Figure 38 MCR terminal 1+0

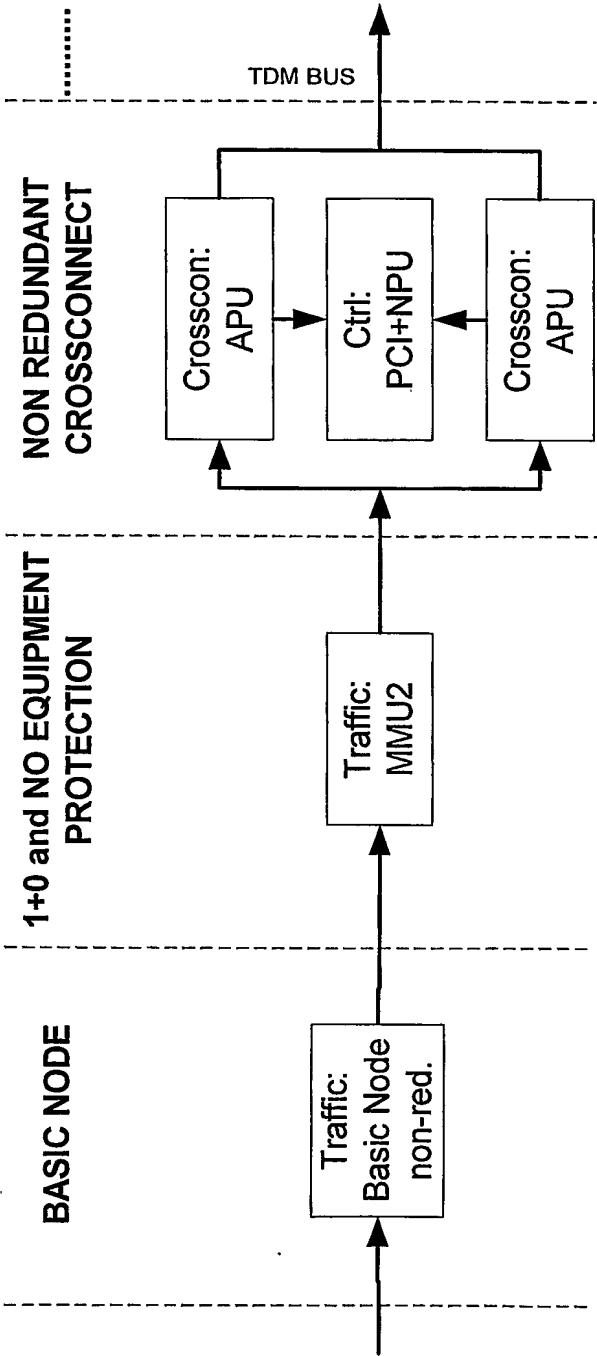


Figure 39 STM-1 terminal 1+1

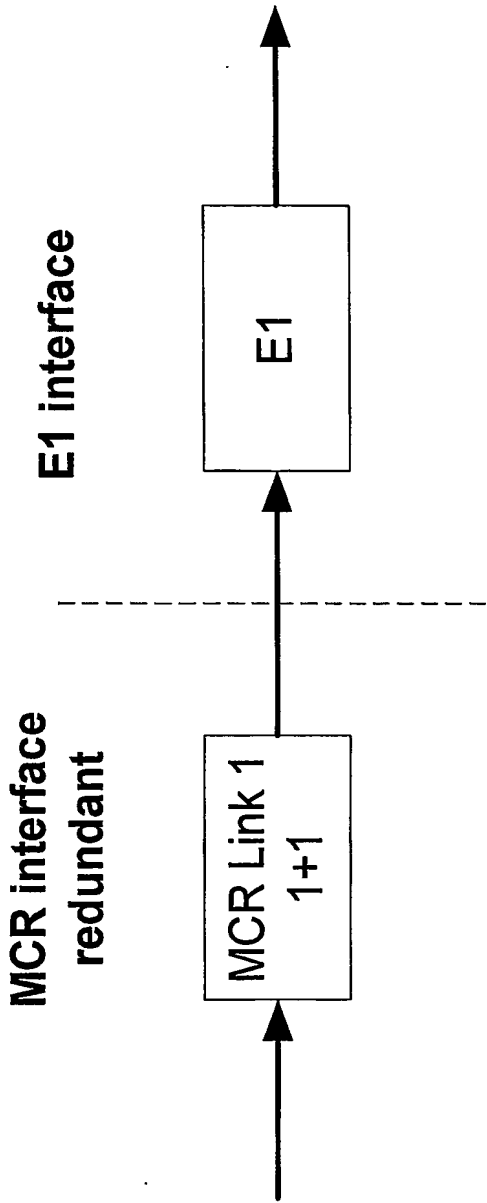


Figure 40 STM-1 terminal 1+0

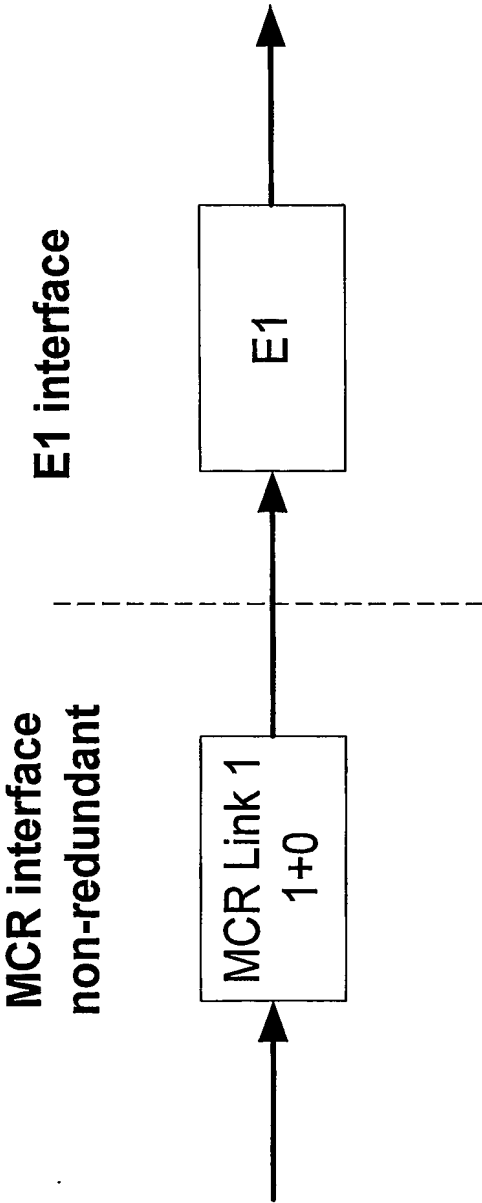


Figure 41 E1 terminal 1+1

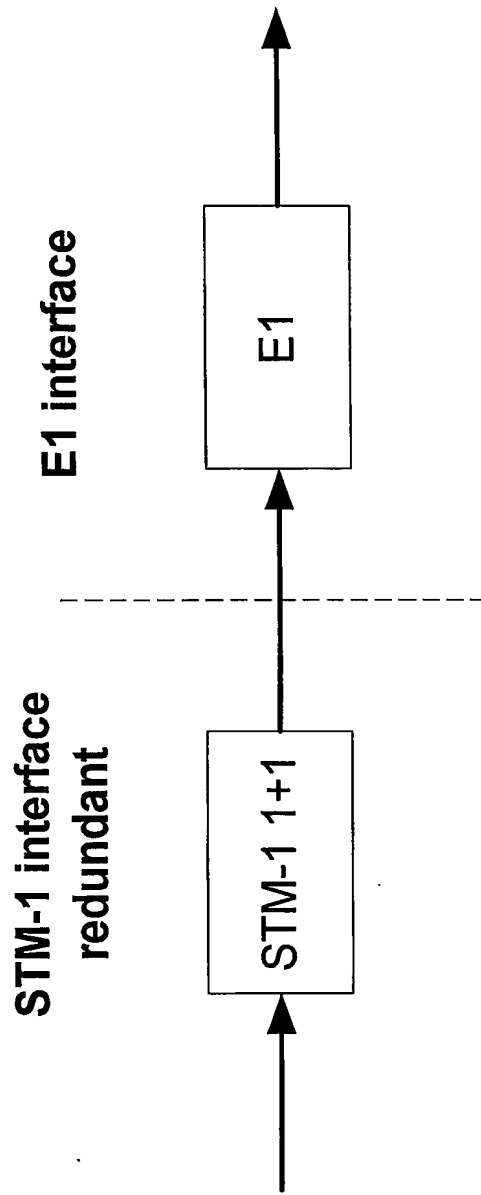


Figure 42 E1 terminal 1+0 (SNCP)

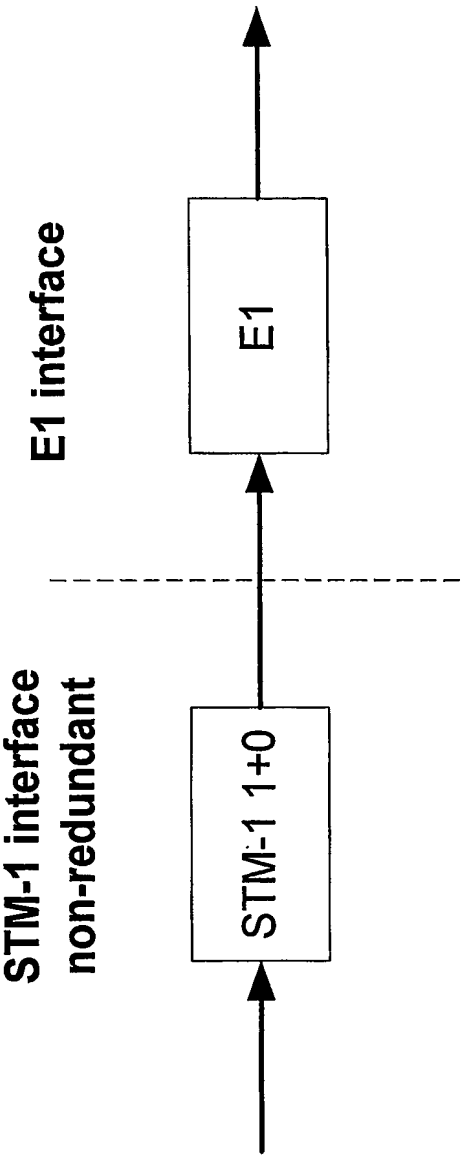


Figure 43 Install new node

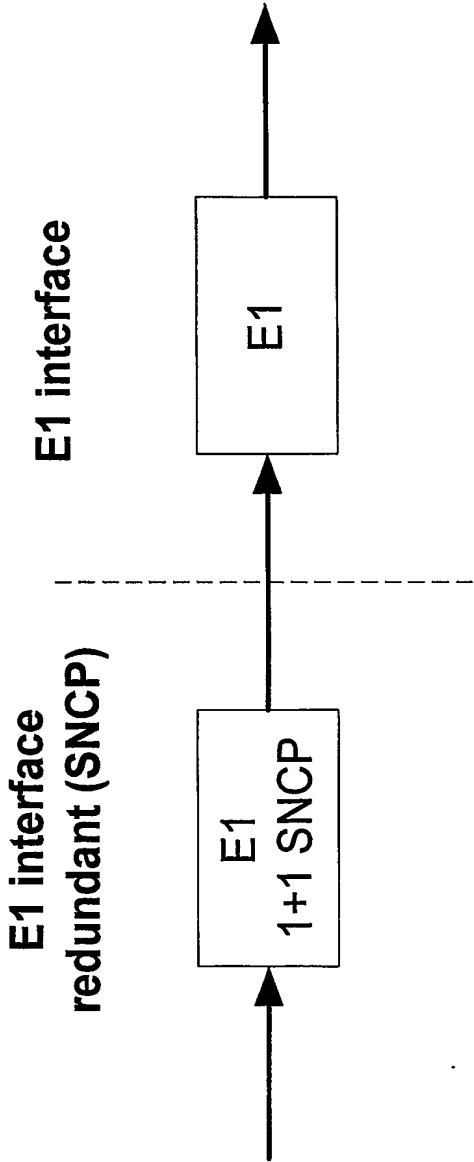


Figure 44 Repair NPU

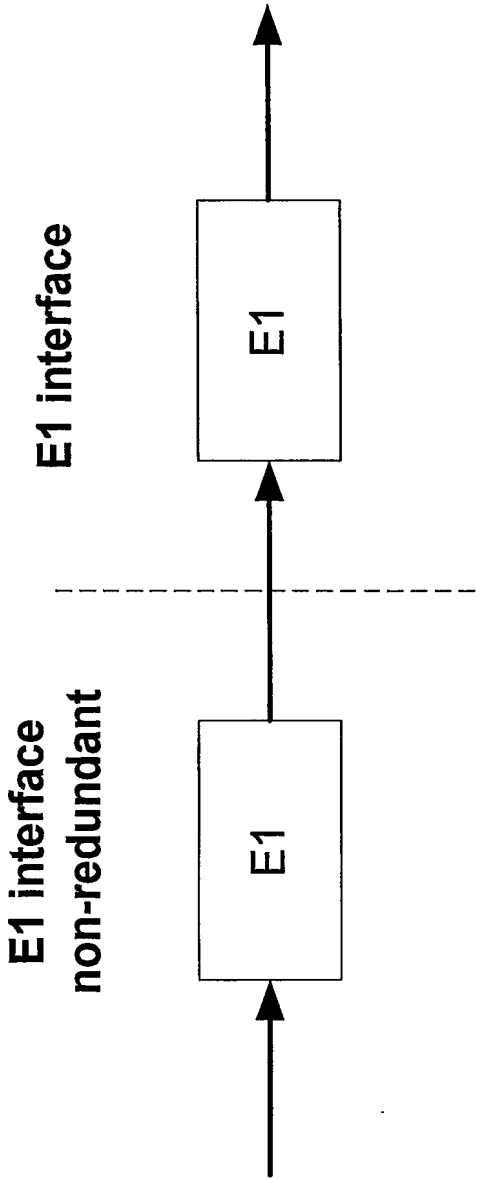


Figure 45 Change forgotten password

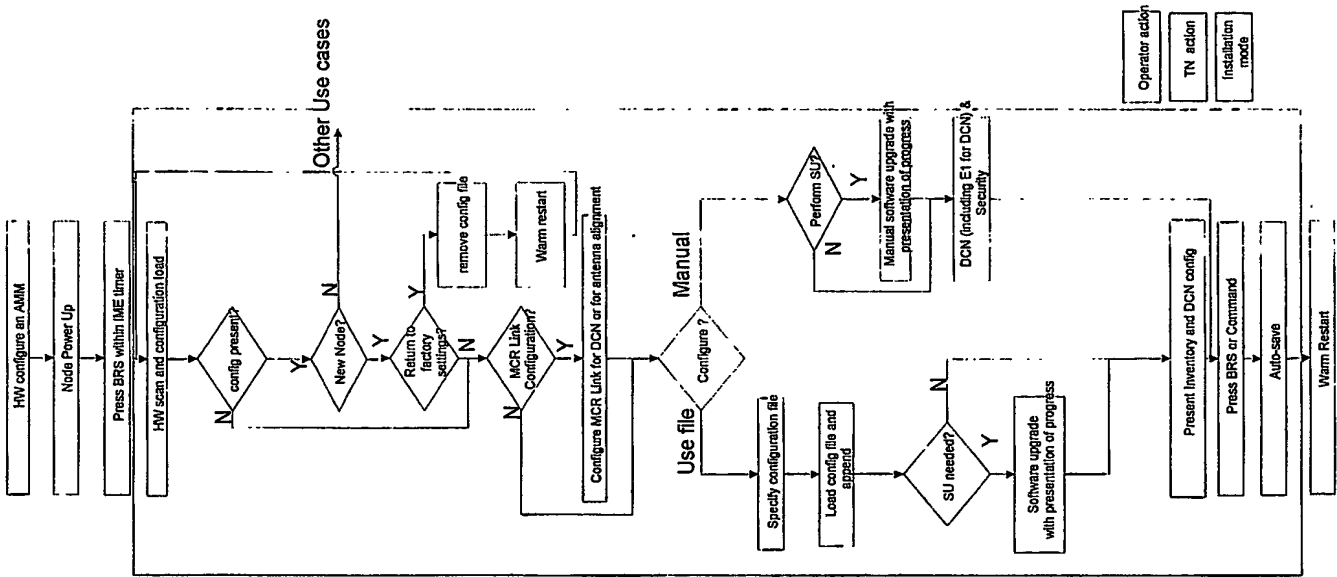


Figure 46
Emergency fallback NPU

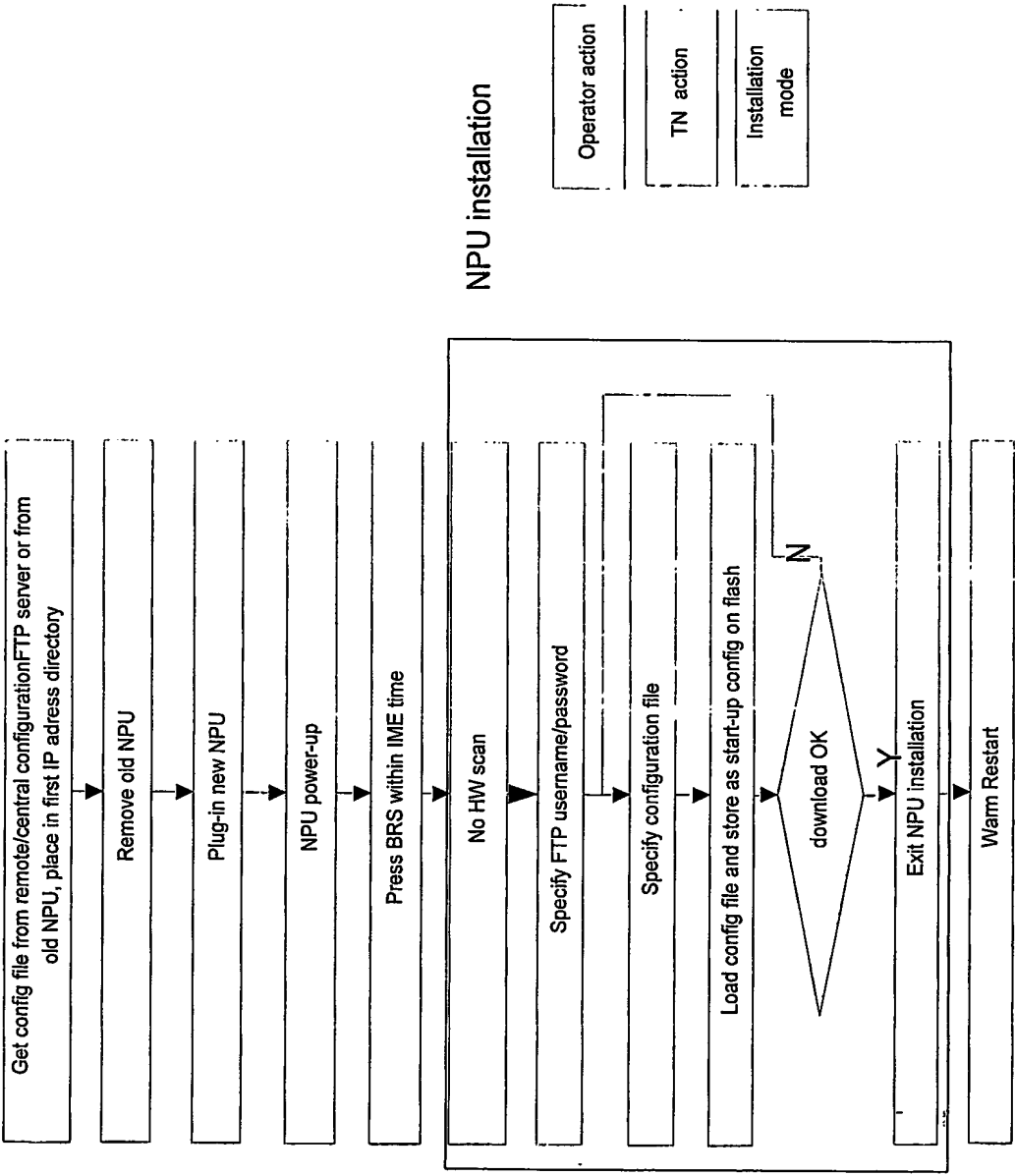


Figure 47 Removal of board (for information only)

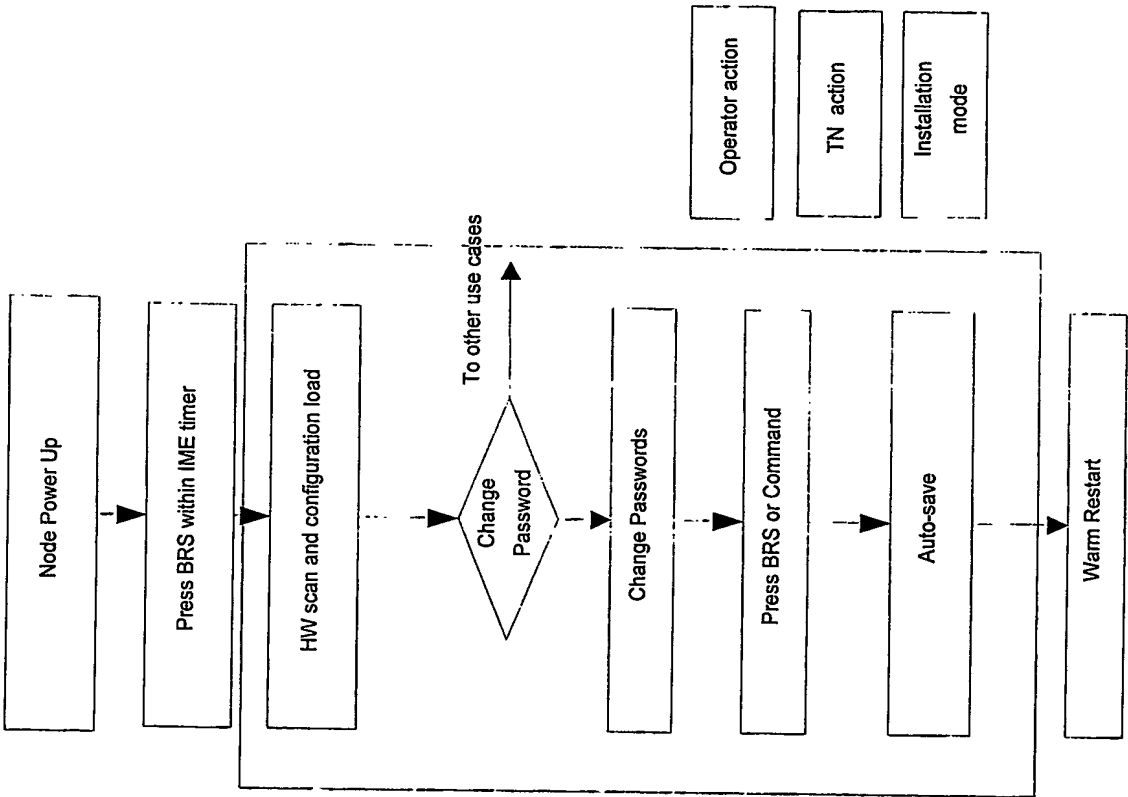


Figure 48 Fault handling of hardware and software error.

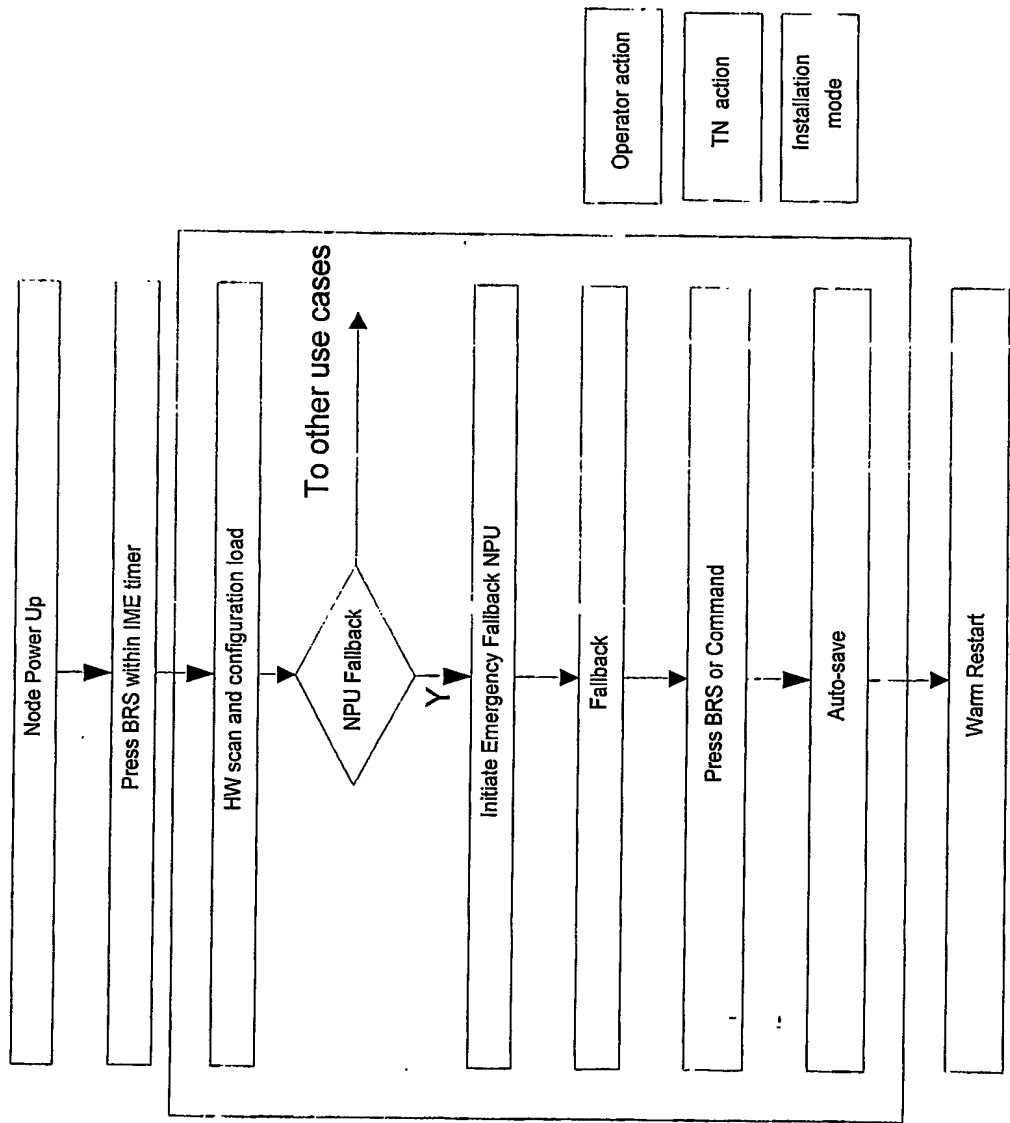


Figure 49 TN Handling of node error.

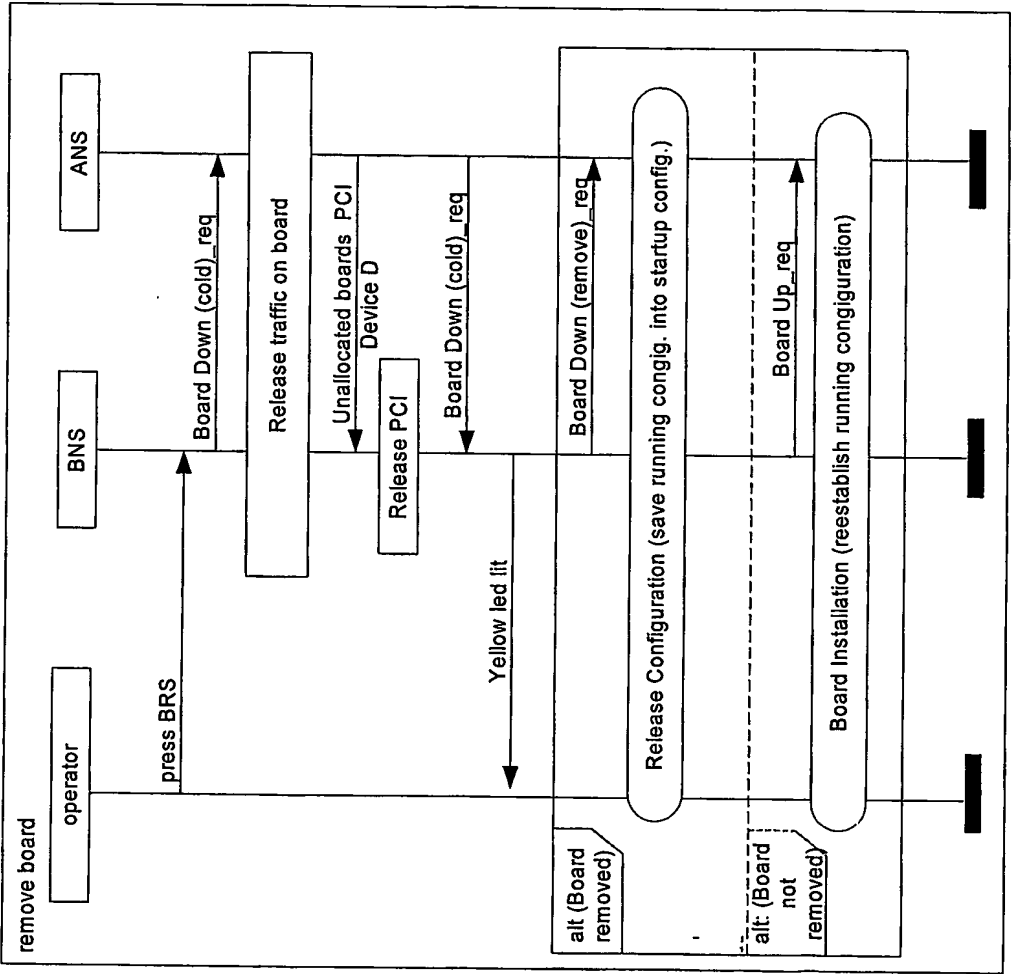


Figure 50 TN Handling of APU/PIU errors.

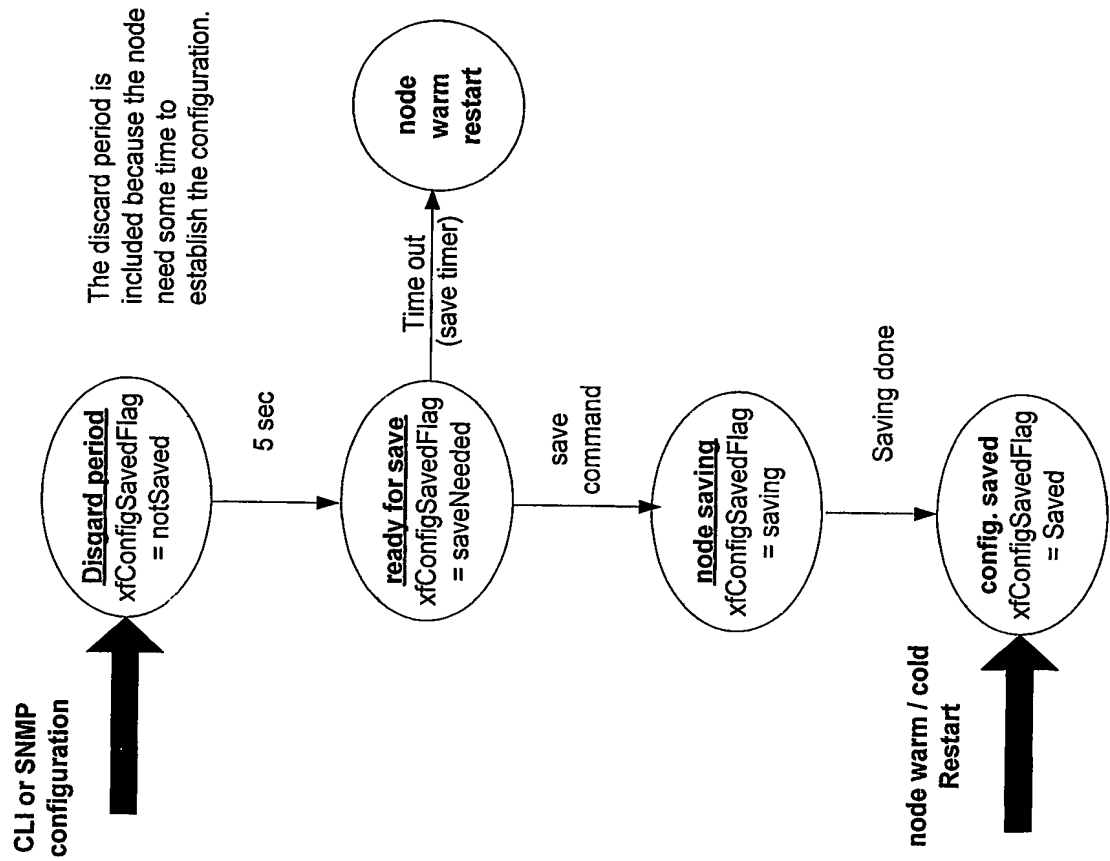


Figure 51 example of TN System Release structure

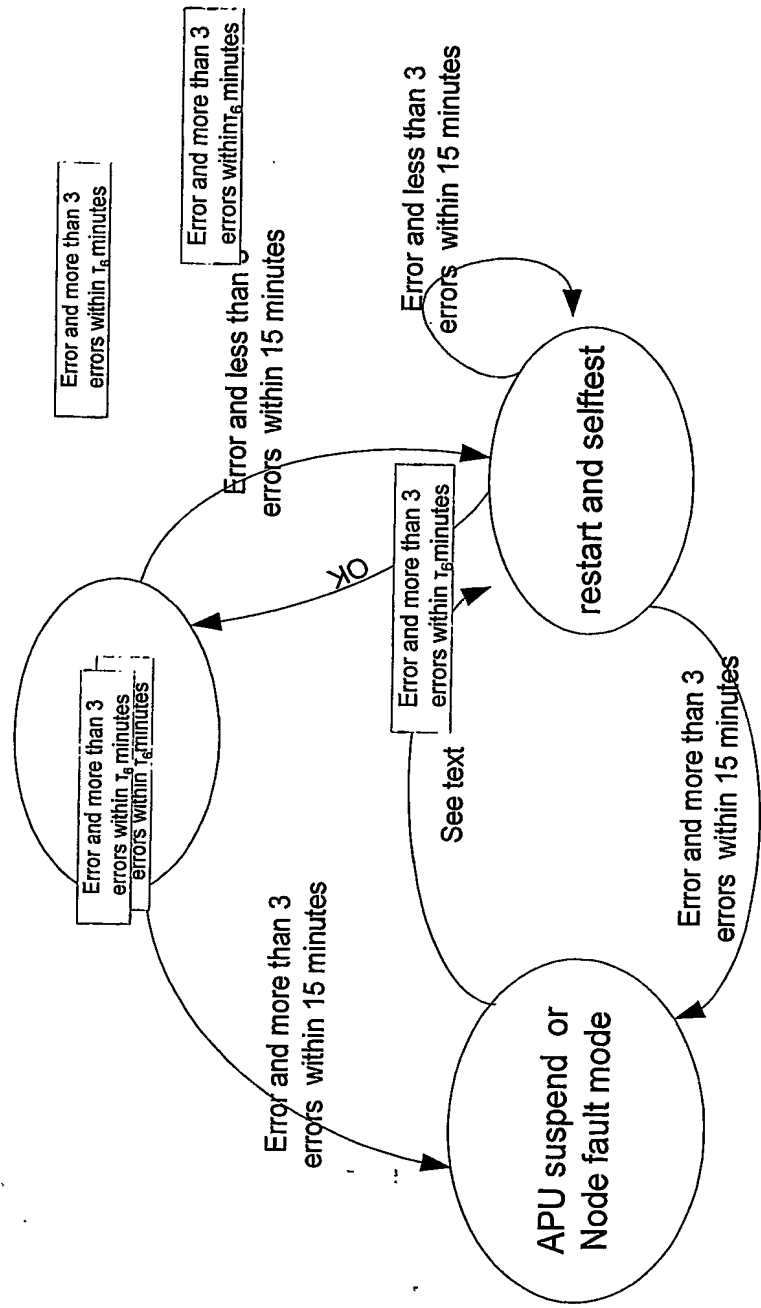


Figure 52 Illustration of the various contents of the APU/NPU memory banks

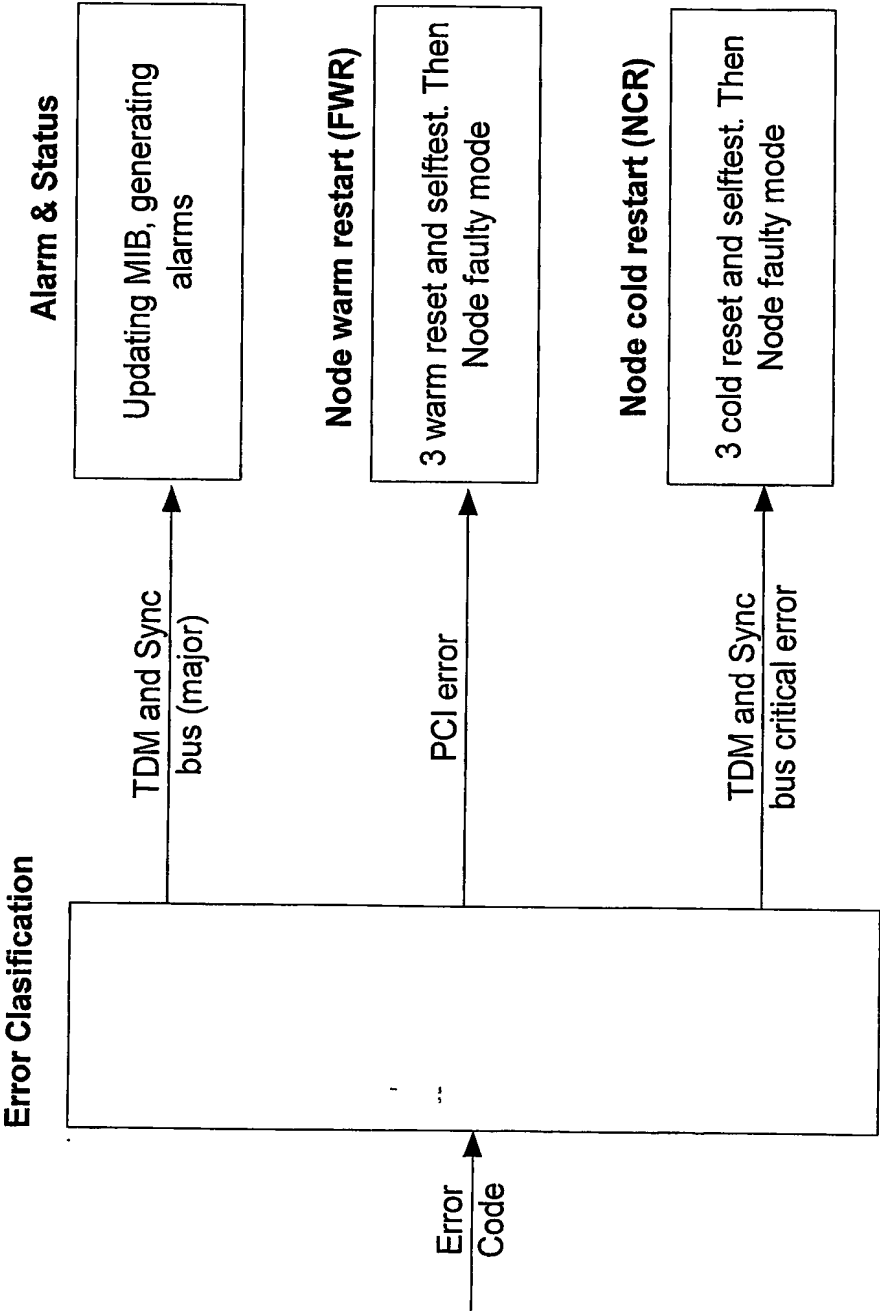


Figure 53 The Software Upgrade process illustrated

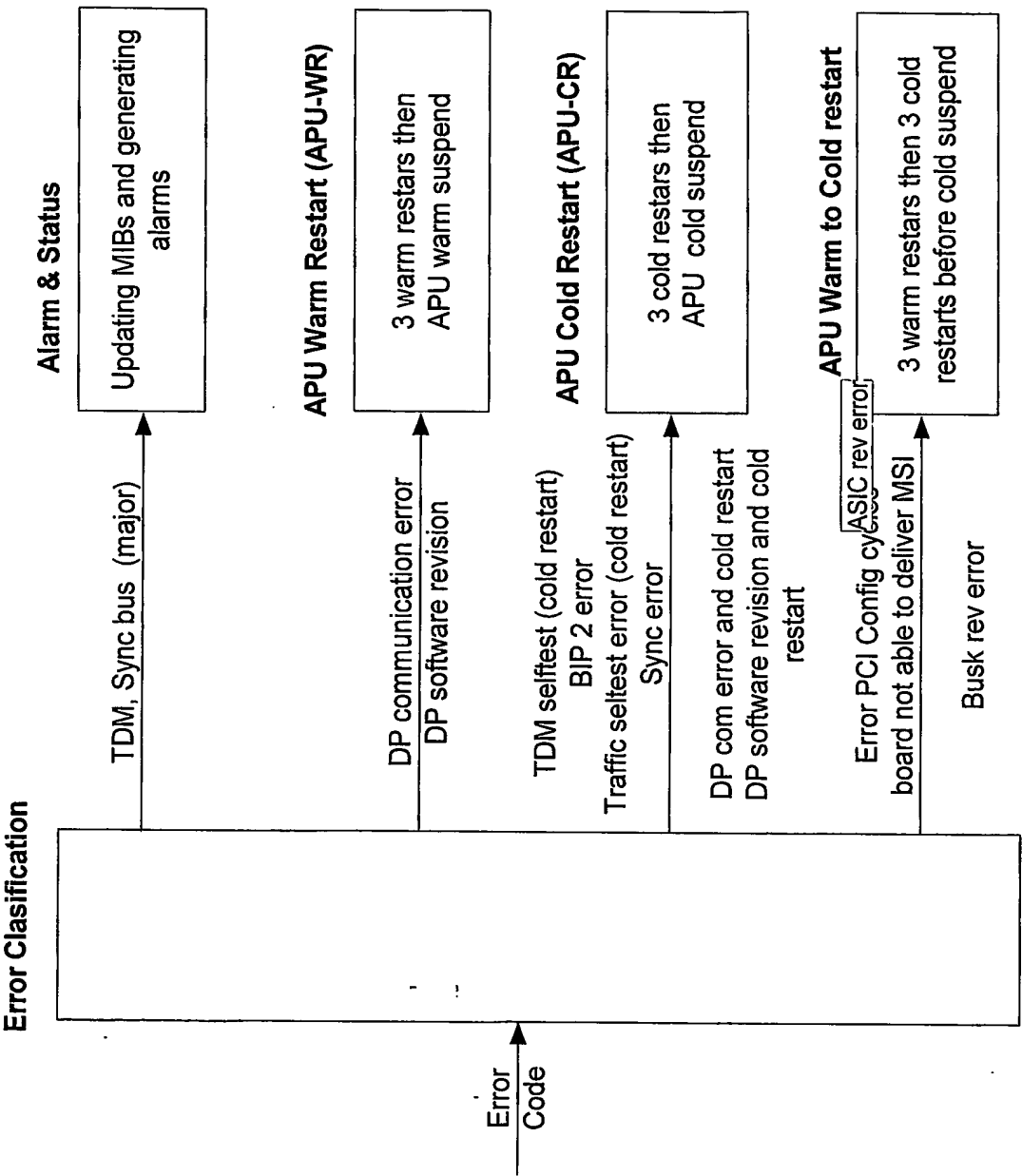


Figure 54 Su of a single APU due to a APU restart

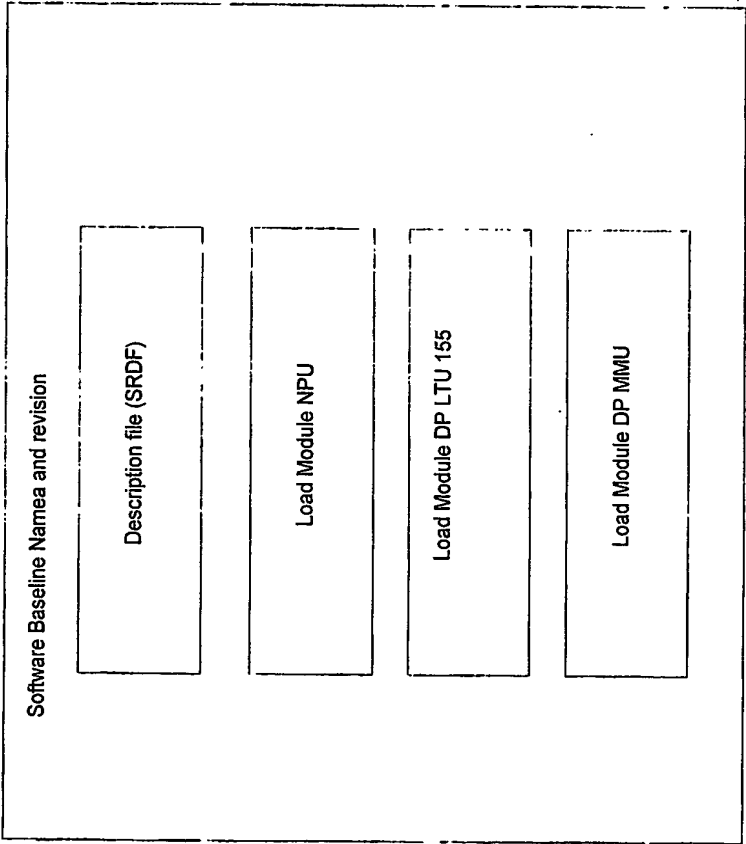
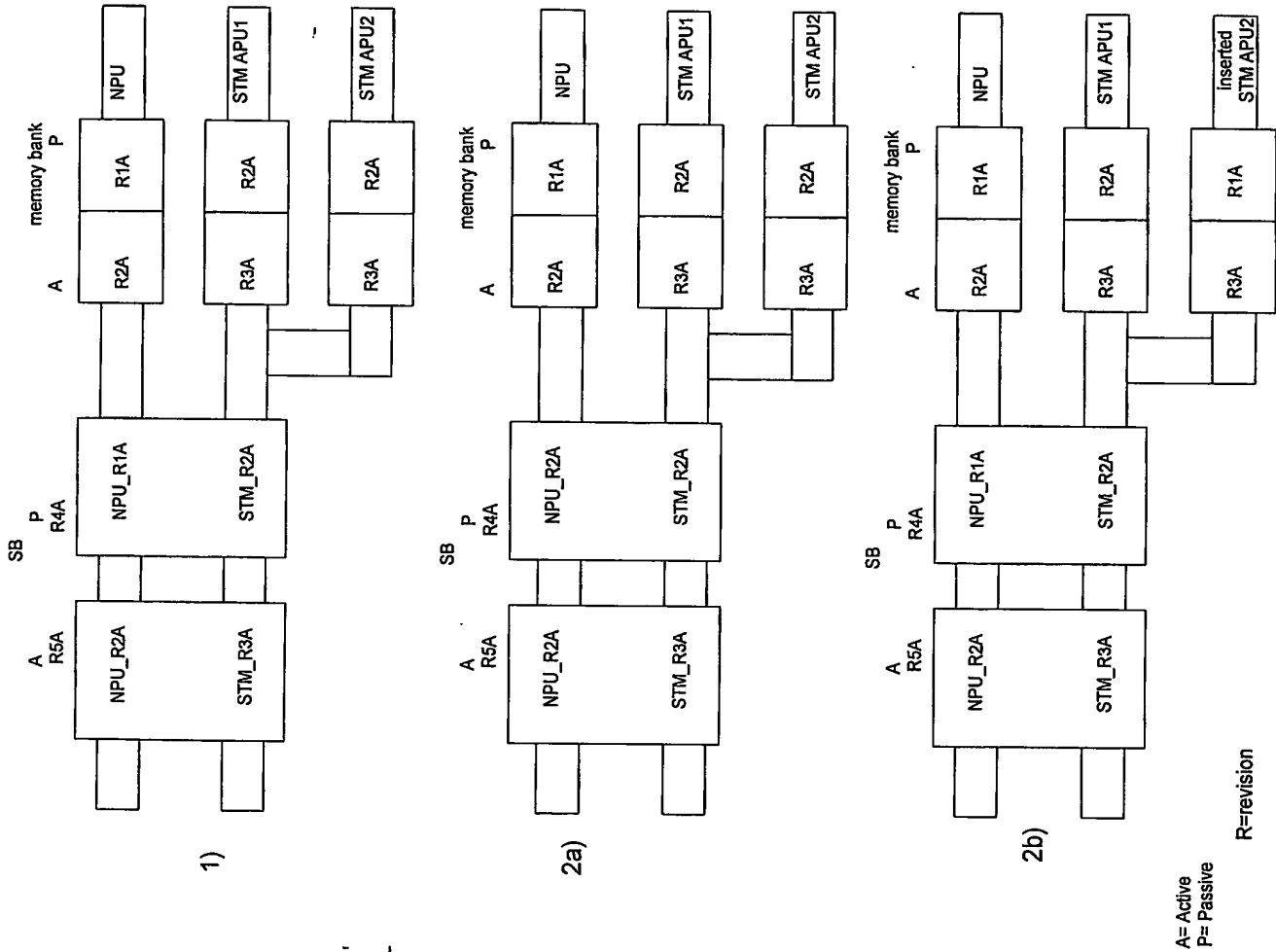
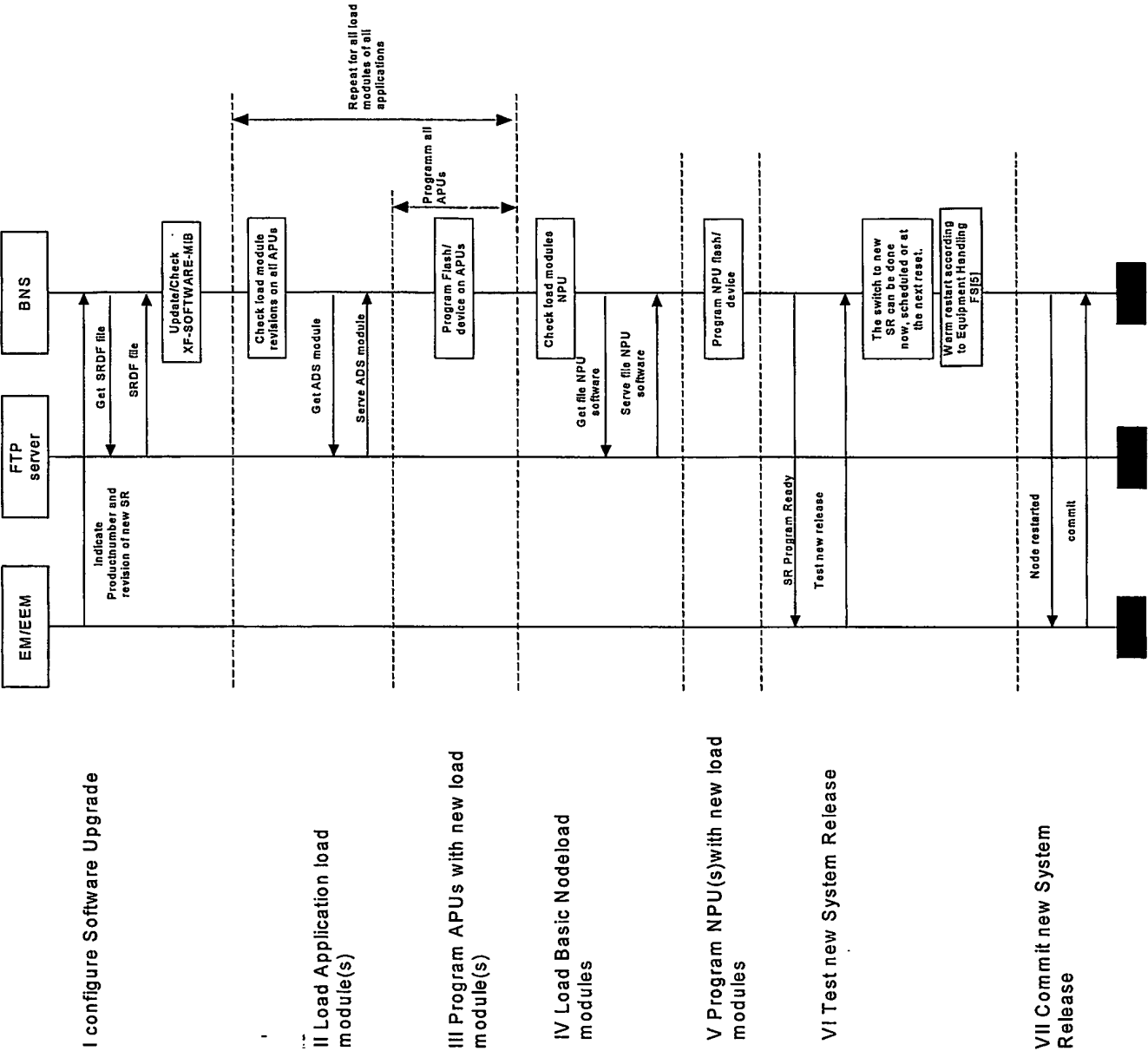


Figure 55 Hot Swap Software Upgrade





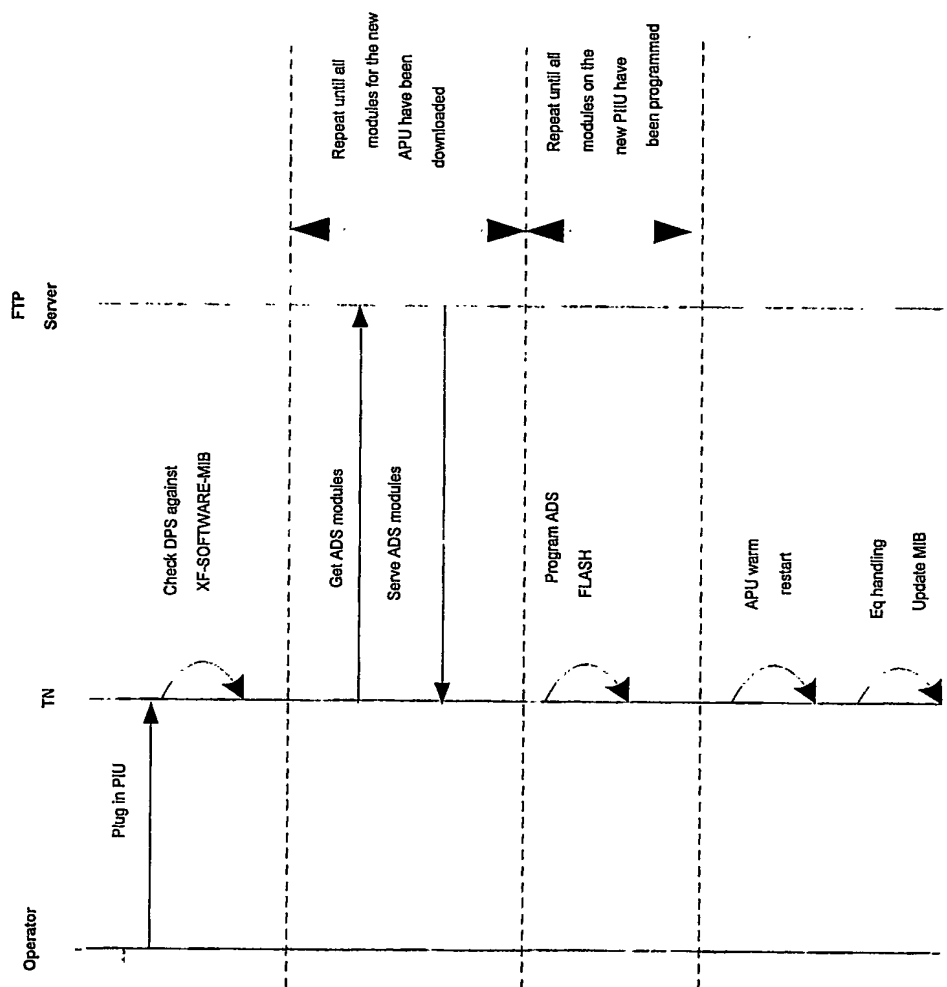


Figure 58

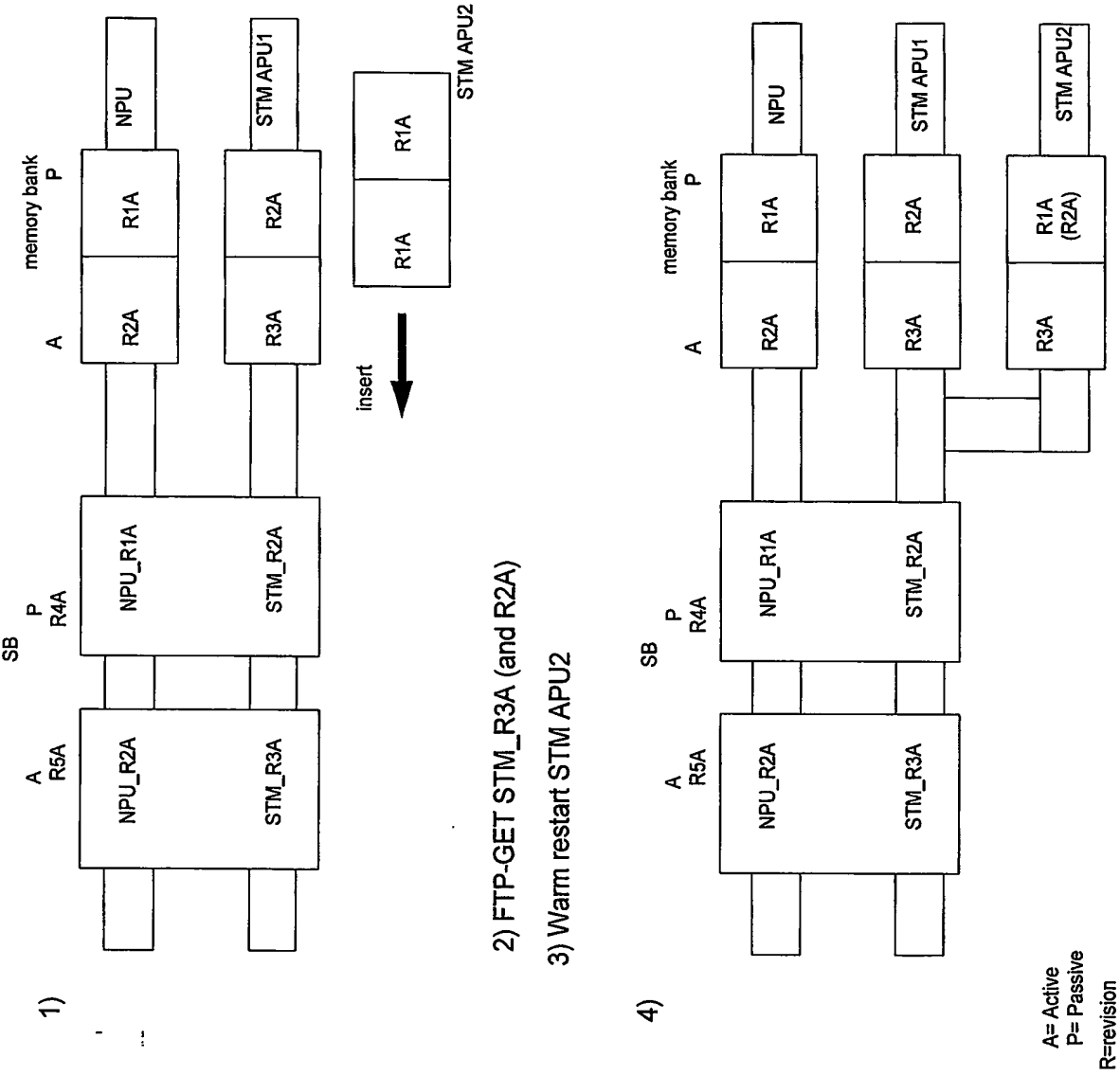


Figure 59

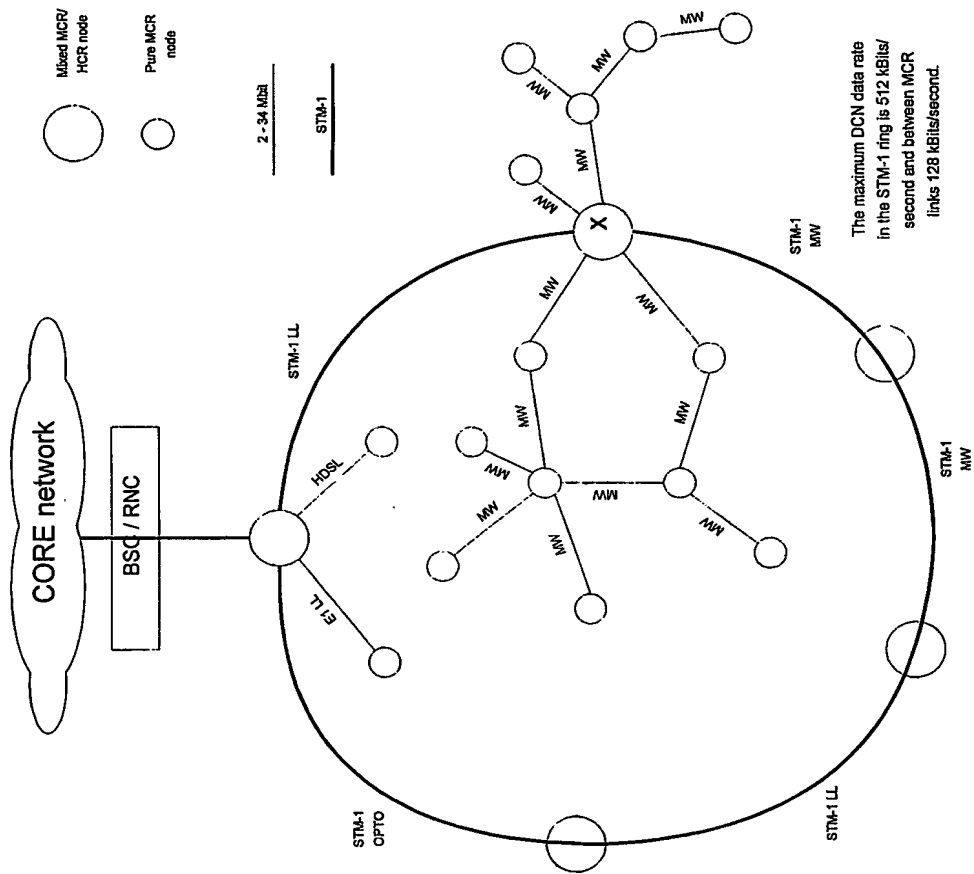


Figure 60